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Hardware reduction in delta-sigma digital-to-analog converters via bus-splitting

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Abstract–This paper discusses a bus-splitting technique for hardware reduction in error feedback digital delta-sigma modulators (DDSMs). The technique is based on error masking and is applied to DDSMs with sinusoidal inputs. We consider the components that contribute to the output signal-to-noise ratio in conventional DDSMs and review new architectures for implementing the digital algorithms without sacrificing performance.

I. Introduction

Delta-sigma modulators are widely used in the implementation of high performance analog-to-digital converters (ADCs), digital-to-analog converters (DACs), digital pulsewidth modulators (DPWMs), all-digital phase locked loops (ADPLLs), and fractional-N frequency synthesizers. These modulators can be classified into three broad categories: (i) continuous-time continuous-amplitude modulators, which are implemented using continuous-time analog filters; (ii) discrete-time continuous-amplitude modulators, which are implemented using switched capacitor filters, and (iii) discrete-time discrete-amplitude modulators (denoted DDSM), which are implemented using digital filters [1], [2]. DDSMs differ from their analog counterparts in that they don't suffer from implementation imperfections and realize their signal processing algorithms with complete accuracy [3].

Publications dealing with analog delta-sigma modulators dominate the literature despite the fact that DDSMs are at least as important as their analog counterparts in terms of commercial applications [4]. In a DDSM, a high resolution discrete-time input is oversampled and requantized to produce a lower resolution output. This coarse requantization takes place within a negative feedback loop such that the resulting quantization noise power is attenuated in the signal band of interest. Ideally, the quantization noise introduced by the DDSM is white and uncorrelated with the DDSM's input. In practice, however, the quantization error often forms short and repeating patterns, and therefore gives rise to spurious tones (spurs) in the output spectrum. The primary stochastic technique used to whiten the spectrum of the quantization noise is the addition of a 1-bit dither sequence to the LSB of the DDSM input [5], [6]. This LSB dithering technique has been shown theoretically to eliminate spurious tones in the DDSM's output spectrum when the DDSM employs two or more integrators in the forward path and the quantizer does not overload [4], [7].

In this paper, we focus on a DDSM for a DAC application [8]. The design of a DDSM for use in an oversampling DAC involves a number of trade-offs. Any internal DAC nonlinearity can cause increased signal distortion and noise at the output. The main advantage of one-bit DDSMs is the inherent linearity of the corresponding one-bit DAC. These modulators are not suitable for high speed data conversion because large oversampling ratios are required to achieve high resolution when the signal bandwidth of interest becomes large [9]. A large OSR restricts the circuit's bandwidth and increases its power dissipation. In addition, it is crucial that the quantization noise introduced by the DDSM is asymptotically white and independent of the modulator's input as spurious correlations between the modulator input and quantization noise can lead to spurious tones in the output spectrum of the DDSM. In data converter applications, spurious in-band tones are undesirable as they degrade the SNR. In the case of one-bit modulators, the white noise approximation is generally not valid.

The use of a multibit DDSM reduces the OSR required to achieve a specific resolution. Multibit modulators produce fewer spurious tones and lower out-of-band quantization noise; this relaxes the analog post filtering requirements [10]. The main disadvantage of a multibit DDSM is the nonlinearity of the corresponding multibit DAC. This necessitates the use of dynamic element matching (DEM) techniques to correct the nonlinearity and ensure that mismatches among the DAC elements do not corrupt the desired signal [11], [12]. In this paper, we focus on multibit digital delta-sigma modulation.

In order to ensure high performance, it is necessary to use high order modulators to obtain significant noise shaping in the signal band. High order DDSMs can be realized with interpolative and Multi stAge noise SHaping (MASH) architectures. An n^{th} order interpolative architecture typically incorporates a single quantizer and a single n^{th} order discrete-time filter. For $n > 1$, interpolative modulators employing a one-bit quantizer require signal conditioning around the loop for stability control,

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which reduces the available dynamic range at the input. Applying a full-scale input to a high-order single bit DDSM causes the quantizer to be overloaded frequently, leading to severe distortion at the DDSM's output. The use of a multibit quantizer increases the achievable dynamic range for a higher order modulator by ensuring its stability over a larger input range [9]. In this work, we focus on the error feedback modulator architecture which is the most efficient implementation of a delta-sigma modulator for a digital application. Prior work [13] has shown this architecture is guaranteed to be stable if an Lth-order FIR noise transfer function (NTF) is used in conjunction with an $(L+1)$-bit truncator.

A number of schemes have been proposed to reduce the hardware requirements of conventional DDSMs. In [15], a first-order DDSM was added in front of the input to a third-order modulator; this preprocessor reduces the overall hardware complexity and the overall system provides a single-bit output. A design methodology based on error masking has been developed and applied to single-quantizer (SQ) and MASH DDSMs, reducing the hardware requirement by up to 20% without sacrificing performance [16], [17]. More recently, the authors of [21] have developed a design technique for implementing the bank of post-processing filters in MASH DDSMs by recoding the carry output signals from the accumulators. This scheme reduces the hardware complexity of the noise cancellation network and can be used in conjunction with error masking, which reduces the hardware complexity of the accumulators, to achieve even lower complexity MASH DDSMs.

In this work, we investigate a bus-splitting idea for implementing dithered DDSMs, in which the digital input word to a high order DDSM is partitioned into a number of parts and the LSBs are processed by one or more low order DDSMs before being recombined with the MSBs. Our work is inspired by the ideas of Norsworthy *et al.* [8] in which the data path of a multibit digital noise shaper is reduced by noting that noise shaping only needs to be performed on the lower few LSBs of an oversampled digital signal in order to be effective. The authors of [8] presented simulation results in which they compared the performance of a traditional single-stage noise shaper with their minimal multibit noise shaping architecture. They truncated the lower 8 bits of a 16-bit sine wave and passed the 8 LSBs through a second-order noise shaper before recombining them with the 8 MSBs. This was shown to produce a similar baseband noise floor to the traditional method of passing the entire 16 bits through the second order noise shaper. Schreier and Temes claim that the accuracy of this architecture can be satisfactory for sufficiently large OSR [2].

To date, the performance of bus-splitting combined with digital delta-sigma modulation has been evaluated based on insight, empirical observations and simulations. The goal of this paper is to formalize the method. Previous work has addressed this method in the context of fractional-N PLLs where the input to the modulator is either a dithered or undithered constant [18]–[20]. In this paper, we consider the components that contribute to the output signal-to-noise ratio (SNR) in the case of a sinusoidal input and show how these can be manipulated to obtain a trade-off between the overall complexity of a modulator and the SNR. Typically, the wordlength of the modulator is defined by the output SNR specification and the wordlength in turn determines the power consumption and area. Reducing the wordlength usually degrades the SNR but decreases the power consumption and area. Spectral shaping and masking techniques have been developed which reduce the hardware requirements faster than the SNR; these can yield a more efficient design from the perspectives of power and area.

II. Conventional Error Feedback Modulator Architecture

Fig. 1(a) shows the block diagram of an l^{th} order error feedback modulator (EFMl) with integer valued signals $x[n]$, $v[n]$, $y[n]$, and $-e[n]$. The input to the modulator is a digital word with N bits. The truncation quantizer in the EFM implements the following operation:

$$y[n] = \left\lfloor \frac{v[n]}{M} \right\rfloor, \tag{1}$$

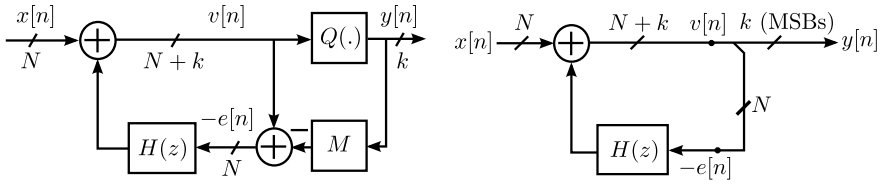
where $\lfloor x \rfloor$ denotes the largest integer less than or equal to x and $M = 2^N$ is the step size of the quantizer. In the Z-domain, we can write the output of the EFM $Y(z)$ in terms of the input $X(z)$ and the quantization error $E(z)$ as

$$Y(z) = STF(z)X(z) + NTF(z)E(z), \tag{2}$$

where $STF(z)$ and $NTF(z)$ are the signal and noise transfer functions, respectively. Assuming the feedback filter is of the form $H(z) = 1 - (1 - z^{-1})^l$, the output is given by

$$Y(z) = \frac{1}{2^N}X(z) + \frac{1}{2^N}(1 - z^{-1})^l E(z). \tag{3}$$

Fig. 1(b) shows the hardware implementation of the EFMl. The k-bit quantization is achieved by taking the k MSBs of $v[n]$. The discarded LSBs, representing the negative of the quantization error ($-e[n]$), are fed back and summed with the input. An EFM is guaranteed to be stable provided that a k-bit truncator is used in conjunction with a $(k-1)^{th}$ order loop filter [13].



(a) Block diagram of an l^{th} order error feedback modulator (EFMl) .

(b) Hardware implementation.

Fig. 1. (a) Block diagram of an l^{th} order error feedback modulator (EFMl) and (b) its hardware implementation

III. DDSM WITH SINUSOIDAL INPUT

A. Oversampled Quantized Sinusoid applied to a DDSM

Consider a signal x with bandwidth f_B that is sampled at a frequency f_s and then quantized using an N-bit quantizer with a quantization step Δ. Assuming a full-scale sinusoidal input, the powers of the signal and quantization noise in the signal band of interest are given by [22]

$$P_{sin} = \frac{(\Delta \cdot 2^N)^2}{8}, \tag{4}$$

$$P_Q = \frac{\Delta^2}{12 \cdot \text{OSR}}, \tag{5}$$

respectively, where OSR is the oversampling ratio defined by $\text{OSR} = \frac{f_s}{2f_B}$. The SNR is defined by

$$SNR = \frac{P_{sin}}{P_Q}. \tag{6}$$

Substituting (4) and (5) into (6) gives

$$SNR = 2^{2N}\left(\frac{12}{8}\right) OSR. \tag{7}$$

The corresponding SNR in dB is given by

$$SNR_{dB} = 6.02N + 1.76 + 3.01 \log_2 OSR. \tag{8}$$

The effective-number-of-bits (ENOB) is defined by

$$ENOB = \frac{SNR_{dB} - 1.76}{6.02}. \tag{9}$$

Substituting (8) into (9) gives

$$ENOB = N + 0.5 \log_2 OSR. \tag{10}$$

Next, consider a signal x with bandwidth f_B that is sampled at a frequency f_s and then quantized using an N-bit quantizer with a quantization step Δ to produce an output x_B. Assume that the signal x_B is applied to an l^{th} order DDSM. We can write the z-transform of the output, $Y(z)$, of the DDSM in terms of the input $X_B(z)$ and quantization error $\epsilon_Q(z)$ as

$$Y(z) = \frac{1}{2^N} STF(z) X_B(z) + \frac{1}{2^N} NTF(z) \epsilon_Q(z), \tag{11}$$

where $STF(z)$ and $NTF(z)$ are the signal and noise transfer functions, respectively. In our example, the noise transfer function is of the form $NTF(z) = (1 - z^{-1})^l$. In this case, the total power of the in-band quantization noise is given by [2]

$$\begin{aligned} q_{rms}^2 &= \int_0^{f_B} \frac{1}{2^{2N}} (1 - e^{-j2\pi f/f_s})^{2l} \epsilon_{Qrms}^2 df \\ &= \frac{1}{12} \cdot \frac{\pi^{2l}}{(2l+1) OSR^{2l+1}}, \end{aligned} \tag{12}$$

where we have assumed that the DDSM produces additive, white quantization noise. The $STF(z)$ is an all-pass filter in the example considered. Consequently, the SNR at the output of the DDSM is given by

$$SNR = \frac{2^{2N}\left(\frac{12}{8}\right) OSR}{1 + \left(\frac{2^{2N}}{2L+1}\right)\left(\frac{\pi}{OSR}\right)^{2L}}$$

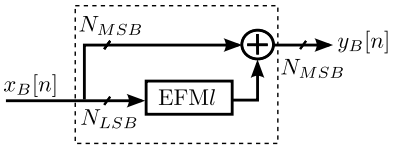
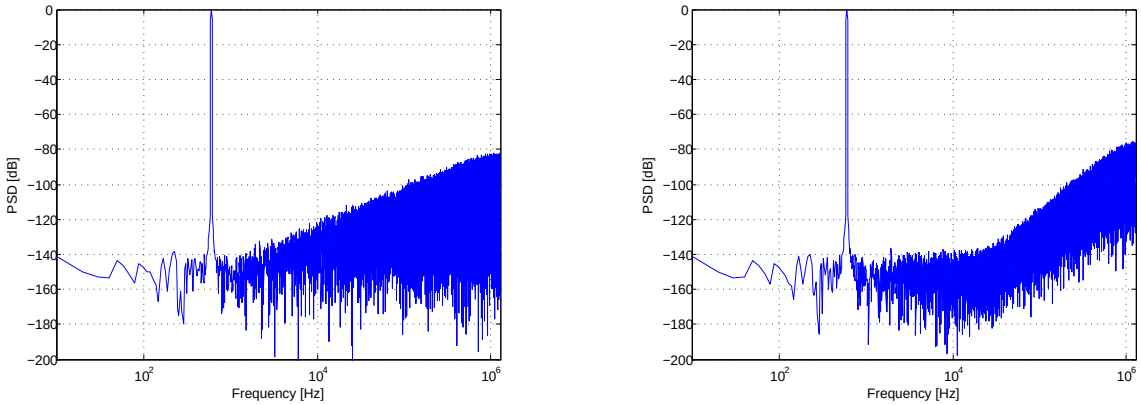


Fig. 2. A quantized input signal x_B is split such that the lower N_{LSB} bits are applied to an l^{th}-order DDSM before being recombined with the upper N_{MSB} bits.



(a) Architecture of Fig. 2 with $l = 1$. The simulated ENOB $= 16$. (b) Architecture of Fig. 2 with $l = 2$. The simulated ENOB $= 18.9$.

Fig. 3. PSDs of a full-scale sinusoid with 20 kHz bandwidth quantized to 16 bits with $OSR = 64$ using the scheme of Fig. 2 with $N_{MSB} = 8$ and $N_{LSB} = 8$ for two different cases; (a) $l = 1$ and (b) $l = 2$. A Hanning window with 2^{18} terms is used when computing the spectrum.

B. Oversampled Quantized Sinusoid applied to a Bus-Splitting DDSM

We consider again a signal x with bandwidth f_B that has been sampled at frequency f_s and quantized by an N-bit quantizer, producing an output x_B. This time, the N-bit word x_B is split so that the lower N_{LSB} bits are first applied to an l^{th} order DDSM, as shown in Fig. 2. The output of this DDSM is combined with the upper N_{MSB} bits to form an N_{MSB}-bit word. Using (13), we can write the SNR of y_B as

$$SNR = \frac{2^{2N}\left(\frac{12}{8}\right)OSR}{1+\left(\frac{2^{2N_{LSB}}}{2l+1}\right)\left(\frac{\pi}{OSR}\right)^{2l}} \tag{13}$$

Comparing (13) with (7), if

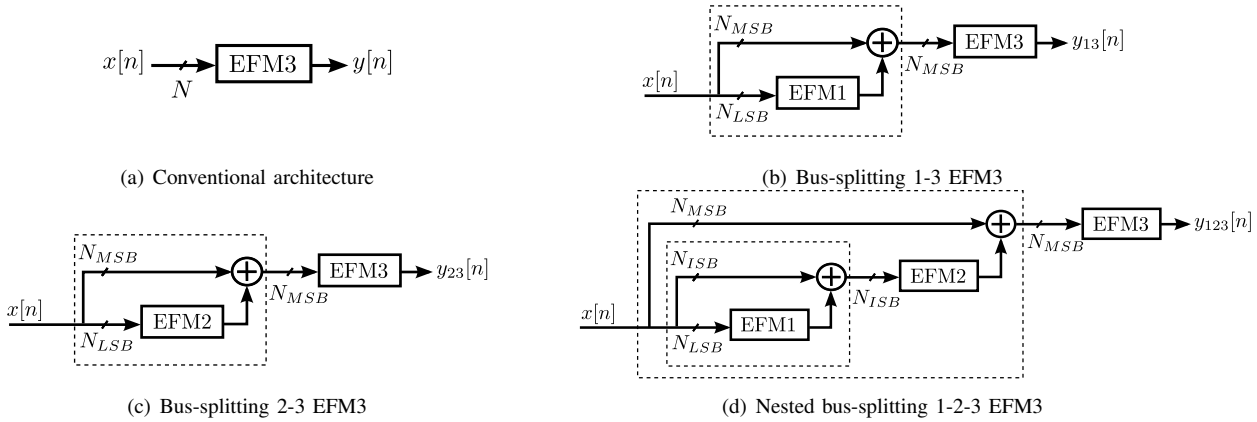
$$\left(\frac{2^{2N_{LSB}}}{2l+1}\right)\left(\frac{\pi}{OSR}\right)^{2l} \ll 1, \tag{14}$$

then the bus-splitting DDSM does not degrade the SNR.

This idea is illustrated graphically in Figs. 3(a) and 3(b), which show the simulated PSDs of a 16-bit full-scale sinusoid with 20 kHz bandwidth using the scheme of Fig. 2 for two different cases; (a) $l = 1$ and (b) $l = 2$. The digital word is split such that the lower 8 bits are applied to a low-order EFM and the output is combined with the upper 8-bits. The simulated ENOB values obtained using the technique described in [23] for cases (a) and (b) are 16 and 18.9, respectively. Note using (9) that ENOB $= 19$ for the original sinusoid. Depending on the choice of l and the partitioning of the input word, a reduction in the wordlength of the sinusoid can be achieved with or without significantly degrading the quality of the output. For the above parameters, using $l = 1$ results in a reduction in the ENOB by 3 bits but the reduction is negligible when $l = 2$. We have developed a design methodology based on error masking [16] which rigorously quantifies the effects of the various parameters on the output ENOB.

IV. Bus-Splitting Architectures

Fig. 4(a) shows the block diagram of a conventional N-bit third-order error feedback modulator (EFM3). In this case, the EFM3 processes the entire N bits of the input. Consider the architectures of Figs. 4(b) and 4(c), which to we will refer as a bus-splitting 1-3 EFM3 and bus-splitting 2-3 EFM3, respectively. In these cases, the digital input word is divided into two



(a) Conventional architecture

(b) Bus-splitting 1-3 EFM3

(c) Bus-splitting 2-3 EFM3

(d) Nested bus-splitting 1-2-3 EFM3

Fig. 4. Block diagrams of the conventional and bus-splitting EFM architectures

parts; the N_{MSB} most significant bits and the N_{LSB} least significant bits. The N-bit input can be written as

$$X = X_{MSB} \cdot 2^{N_{LSB}} + X_{LSB}, \tag{15}$$

where X_{MSB} and X_{LSB} correspond to the MSBs and LSBs, respectively, and

$$N = N_{MSB} + N_{LSB}. \tag{16}$$

Consider the bus-splitting architecture of Fig. 4(d), to which we will refer as a *nested* bus-splitting 1-2-3 EFM3. In this case, the digital input word is again divided into two parts: the N_{MSB} most significant bits, and the remainder. The latter is then further subdivided into the N_{ISB} intermediate bits and the N_{LSB} least significant bits. The N-bit input can be written as

$$X = X_{MSB} \cdot 2^{N_{LSB}+N_{ISB}} + X_{ISB} \cdot 2^{N_{LSB}} + X_{LSB}, \tag{17}$$

where X_{MSB}, X_{ISB}, and X_{LSB} correspond to the most significant, intermediate, and least significant bits, respectively, and

$$N = N_{MSB} + N_{ISB} + N_{LSB}. \tag{18}$$

Consider a 24-bit digital input word [10]–[12], [24] which is interpolated by a factor of 64 and applied to an EFM3, as shown in Fig. 4(a). The simulated output PSD is shown in Fig. 5(a). The simulated output PSD of the bus-splitting 1-3 EFM3 with $N_{LSB} = 12$ and $N_{MSB} = 12$ is shown in Fig. 5(b). The simulated output PSD of the bus-splitting 2-3 EFM3 with $N_{LSB} = 17$ and $N_{MSB} = 7$ is shown in Fig. 5(c). The simulated output PSD of the nested bus-splitting 1-2-3 EFM3 with $N_{LSB} = 10$ $N_{ISB} = 7$ and $N_{MSB} = 7$ is shown in Fig. 5(d). In all cases, the simulated ENOB ≈ 17.5.

V. Conclusions

In this paper, we have reviewed the conventional error feedback modulator architecture and have introduced a bus-splitting technique for reducing the hardware complexity of DDSMs. Behavioral simulations show that by appropriately partitioning the modulator input word, comparable performance can be achieved with the bus-splitting architecture. A rigorous design methodology and the relative hardware requirements of the various bus-splitting architectures will be reported elsewhere.

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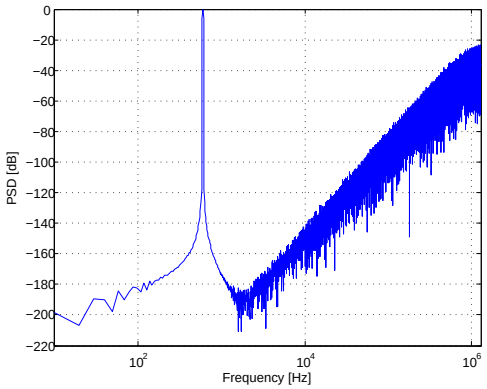
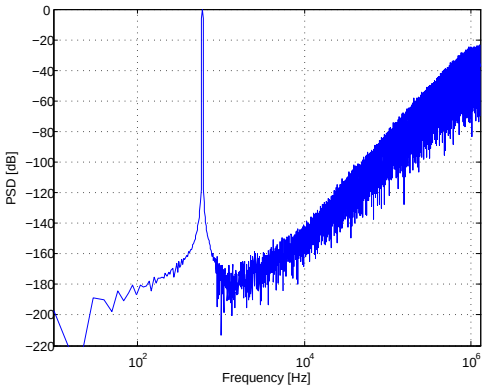
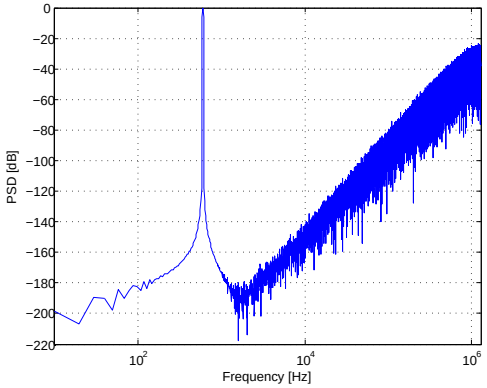


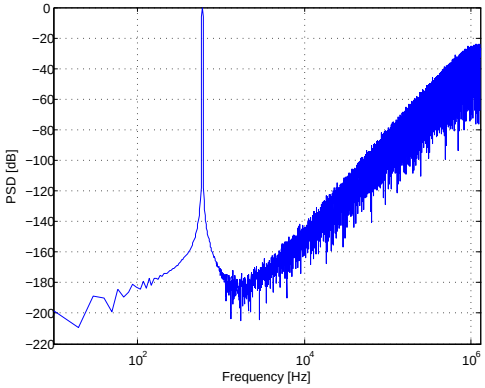
(a) Conventional EFM3 architecture. (Fig. 4(a))



(b) Bus-splitting 1-3 EFM3 with $N_{LSB} = 12$ and $N_{MSB} = 12$. (Fig. 4(b))



(c) Bus-splitting 2-3 EFM3 with $N_{LSB} = 17$ and $N_{MSB} = 7$. (Fig. 4(c))



(d) Nested bus-splitting 1-2-3 EFM3 with $N_{LSB} = 10$, $N_{ISB} = 7$ and $N_{MSB} = 7$. (Fig. 4(d))

Fig. 5. PSDs of (a) the conventional and (b)-(d) bus-splitting EFM architectures

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