

A simplified cascade controlled channels for a 3 – bits discrete pure linear analog preprocessing folding ADC architecture

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Abstract-This is an example for preparing the full paper that is identical with the extended summaries format. It must be written in Times New Roman 10pt and should contain maximum 12 lines; the ‘Abstract’ word is written in Times New Roman 10pt bold italics, with the character spacing expanded by 1pt.

I. Introduction

ADCs based on folding architecture involves the use of two distinct ADCs flash which, working in a structure almost parallel, are able to give almost the same performance as a single ADC flash in terms of speed conversion, but with a drastic lower number of comparators allowing a great savings of power[1,2].

The folding ADC output is a digital word composed of two sections: the most significant bits are given by the first flash converter called “coarse” that digitizes the input signal with low resolution, while the second, called “fine” quantizer gives the least significant ones. The input of the first flash is the signal that must be converted; the difference between the input signal and its digitized version is sent to the fine quantizer, so the input of this second flash converter will always be a value between zero volt and the quantum volt. This voltage difference is realized by an input signal pre-elaborator analogical circuit that is the most critical circuit inside the folding architecture. In literature there are many examples of circuitry that can realize the transfer function necessary to correctly drive the second quantizer[3]. Some configurations are based on current-mirror that can be used to implement piecewise linear transfer characteristic of folding amplifier. The cascade current mirror version is strongly suitable for low voltage low power design, but, to obtain adequate accuracy, the length of transistors have to be large with the disadvantage of low speed[4]. Another technique uses folding amplifier based on hyperbolic tangent transfer function of voltage differential pairs. This scheme solves the bandwidth problem, but it suffers from intrinsic output current distortion that limits the number of folds[5]. Some of these drawbacks are overcome by wired-OR configuration at the differential pair outputs to reduce the common-mode output signal and to provide buffering, but this circuit still suffers from the threshold perturbing effects of a single-ended reference scheme[6]. Other circuits are hard to implement in integrated technology because they require the contemporary use of MOSFETS with the body separated by the source and MOSFETS with body connected to the source. This would oblige to realize silicon isles to separate each transistor from the other parts of the circuit[7,8].

In this paper, a very simple linear folding architecture for subranging ADC is presented. The preprocessing analog structure is constituted with 2^n (with n number of bits) parallel circuits made with a simple subtracting node and with a series of two MOS switches able to join the functionalities of DAC, summing node and amplifier typical of classical subranging ADC. To validate the idea an accurate simulation of the single channels and of the whole structure has been realized.

II. The circuit proposed

The voltages that can be presented to the input of the fine quantizer must be between 0 and the quantum, in a folding architecture, the analog preprocessing circuit allows this operation. The structure can be viewed as composition of sub-circuits called channels in a number fixed by the wanted resolution. So, for a 3-bits stage are necessary 7 channels (2^3-1). A ramp signal that goes from 0 to 5 V is used as the input signal for simulations. The circuit has to be able to output a saw-tooth composed of n little ramps with a range always inside the quantum. In A subsection is analysed the single channel behaviour, while in B subsection the behaviour of the whole circuit.

A. Single channel behaviour

To well understand the whole system it is necessary to explain before the behaviour of a single channel. It's the core of the whole circuit and is composed by a NMOS-PMOS couple connected like in Figure 1. The input voltage is a ramp between 0 and 5 V that covers the A/D full scale. The resistor between the positive supply V_P and the drain of the NMOS has been chosen equal to 100 k Ω to have a very low output current unable to influence the voltage reference T_1 applied on the source, so also lowering the consumptions. A further consideration is joined with the trans-conductance defined as $g_m = i_{out}/V_{in}$, it is clear that lower is the output current, lower it will be the dynamic of the control voltage V_{in} . The NMOS acts as an open circuit up to the V_{GS} is lower than the threshold voltage V_{th} , positive for the NMOS.

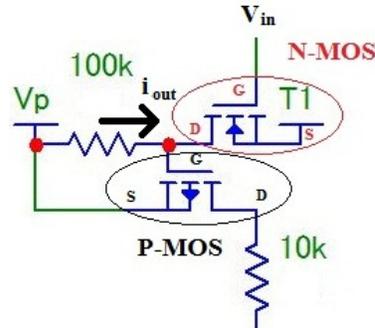


Figure 1. Transistor NMOS-PMOS couple.

When V_{in} overcomes the sum between the threshold voltage V_{TH} and the voltage source T_1 ,

$$V_{in} - T_1 > V_{TH} \rightarrow V_{in} > V_{TH} + T_1 \quad (1)$$

the NMOS switches on passing from the interdiction zone to the linear one allowing the switch on of the PMOS at the same time. The transistors act like a switch that open or close itself in function of the voltages applied V_{in} , supplying through drain resistor a current of 0.5 mA. The aim of the channel is to identify the border between two successive quantum voltages (V_{qn-1} , V_{qn}).

B. Multiple channels circuit for a three bits A/D quantizer

Considering to put in parallel seven NMOS-PMOS couples, it is possible to realize the circuit for a three bits A/D converter as shown in Figure 2.

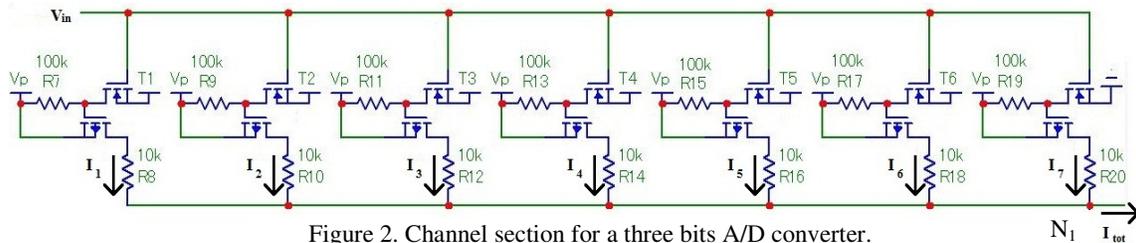


Figure 2. Channel section for a three bits A/D converter.

Each NMOS-PMOS couple has to divide the whole input voltage range in the number of quantum specified for a three bits A/D (eight sub-ranges). To get this, each channel needs of a different voltage reference T_n ($n=1,2,\dots,7$). To simplify the circuit, the reference of the last channel has been connected to mass while the previous ones have a negative reference voltage equal to a progressive multiple of V_q provided by a voltage divider.

In order to progressively switch on the channels, it is necessary to translate the input ramp by a negative voltage offset in such a way to satisfy the next equation :

$$\text{being } V_{in} = V_S + V_{OS}, \text{ when } V_S = nV_q \rightarrow V_{in} + T_n = V_{TH} \quad (2)$$

where V_S is the instantaneous value of the input ramp and V_{OS} the negative offset.

The circuit in Figure 3 allows to obtain V_{in} . By a voltage divider, the supply positive voltage V_P is divided by the resistors R_1 and R_2 . V_1 is applied to the non inverting input of A_1 that acts like a buffer. V_{out} is sum of two voltages:

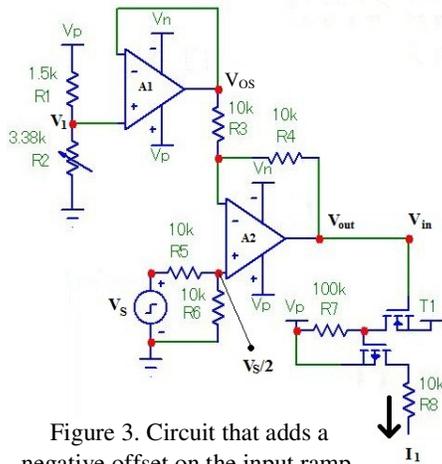


Figure 3. Circuit that adds a negative offset on the input ramp.

$$V_{out} = V_{o1} + V_{o2} \quad (3)$$

$$\text{with } V_{o1} = -(R_4/R_3) V_1 = -V_1 \text{ and } V_{o2} = (1+R_4/R_3) V_S = 2V_S \quad (4)$$

As the gain of the A_2 stage is two for V_S , it has to be divided; the $R_5 - R_6$ voltage divider realizes this operation. The V_{out} of this stage is given by:

$$V_{out} = V_{o1} + V_{o2} = 2V_S R_6 / (R_6 + R_5) - V_{OS} = V_S - V_{OS} \quad (5)$$

Each time that the input signal overcomes a multiple of the quantum voltage, the channels switch on summing a 0.5 mA current each, if the Node N_1 (Figure 2) is a virtual ground. In such a way, an input ramp generates a current staircase on the N_1 node. At this point of our analysis if the input voltage ramp would be converted in a current, it would be possible to subtract it from the staircase. As shown in Figure 4, A_3 stage is used to invert the

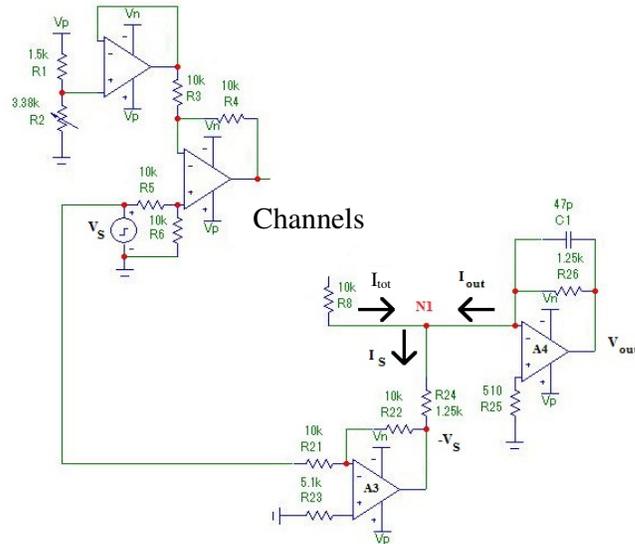


Figure 4. Whole structure of the first channel.

input ramp giving a negative voltage as output ($-V_S$). Exploiting R_{24} , A_3 provides a current I_S that exits from the node N_1 and is subtracted to the I_{tot} . Their difference provides the current I_{out} exiting from the node N_1 .

The A_4 stage realizes the current-voltage conversion $I_{out} \cdot V_{out}$ by the feedback resistor R_{26} of 1,25 k Ω . It maintains a virtual ground to the inverting pin avoiding undesirable voltage drop and undesirable variation of the current. The voltage output of this stage will be:

$$V_{out} = -R_{26} \cdot I_{out} \quad (6)$$

This means that V_{out} , that represents the quantization error, is the subtraction between the voltage generates by I_S on R_{26} and that generates by I_{tot} on the same resistor, or, in other words, the difference between the input voltage V_S and the staircase given by the A/D conversion: it is a saw-tooth voltage

corresponding to the quantization error with an amplitude of 0.625 V for a three bits A/D.

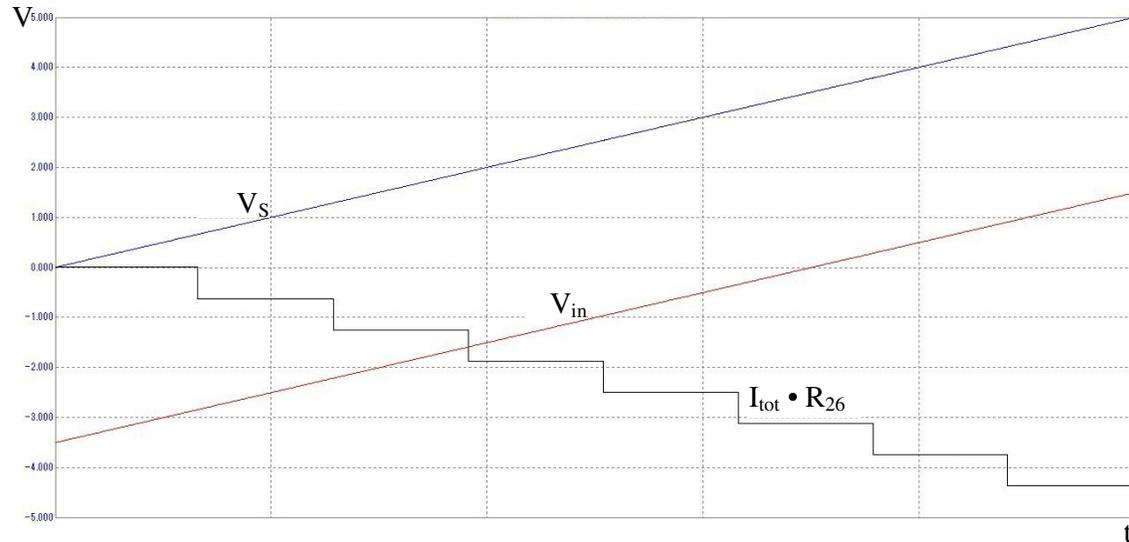


Figure 6. Input voltage trend V_{in} on the gate obtained by the translation of the input voltage V_S and the voltage $I_{tot} \cdot R_{26}$.

Figure 6 shows the input voltage waveform of V_{in} on the NMOS gate obtained by the translation of the voltage V_S to generate the output voltage V_{out} and the product between $-I_{tot}$ and R_{26} . The presence of the A_3 stage allows to invert the input ramp so the voltage V_S , applied to R_{24} , generates an current I_S that exits from N_1 . The equation to this node is: $I_{out} = I_S - I_{tot}$. The output current that fixes the output voltage by the feedback resistor R_{26} is given by the difference between the current generates by $-V_S$ applied to R_{24} and the total current supplied by the active couples. V_{out} will be a saw-tooth voltage correspondent to the quantization error of the A/D conversion. The amplitude levels of each tooth will have a value equal to 0.625 V.

C. Whole circuit for a three bits A/D quantizer

Summarizing, the proposed circuit is shown in Figure 7 and is composed of:

1. a first buffer A_1 that provides V_{OS} ;
2. an operational amplifier A_2 in differential configuration that negatively translates the input voltage V_S .

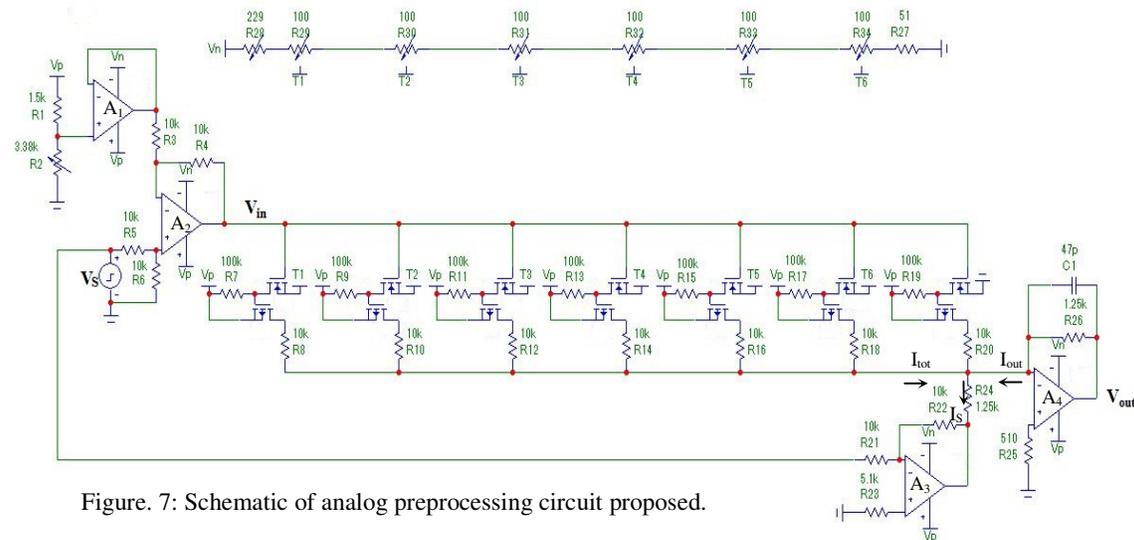


Figure. 7: Schematic of analog preprocessing circuit proposed.

3. 2^N-1 analogical channels realized by MOSFET transistor NMOS-PMOS couples that act as switches that open or close themselves depending on the achievement of a voltage equal to a multiple of the quantum. Every MOSFET transistor couple supplies a 0.5 mA current. In such a way, the channels generate a current staircase (I_{tot}) with a number of stairs equal to the number of quantum overcome by the ADC input signal.
4. The A_3 operational amplifier, in inverting configuration, generates thanks to R_{24} , a current ($-I_S$) proportional to the ADC input voltage. This current has a direction opposed to the current generated by the switches of the previous point.
5. At the end, the A_4 stage is a current-voltage converter that allows the conversion of the output current I_{out} , obtained as subtraction between I_S and I_{tot} , to a voltage between zero and the quantum voltage ready to be converted by the fine quantizer.

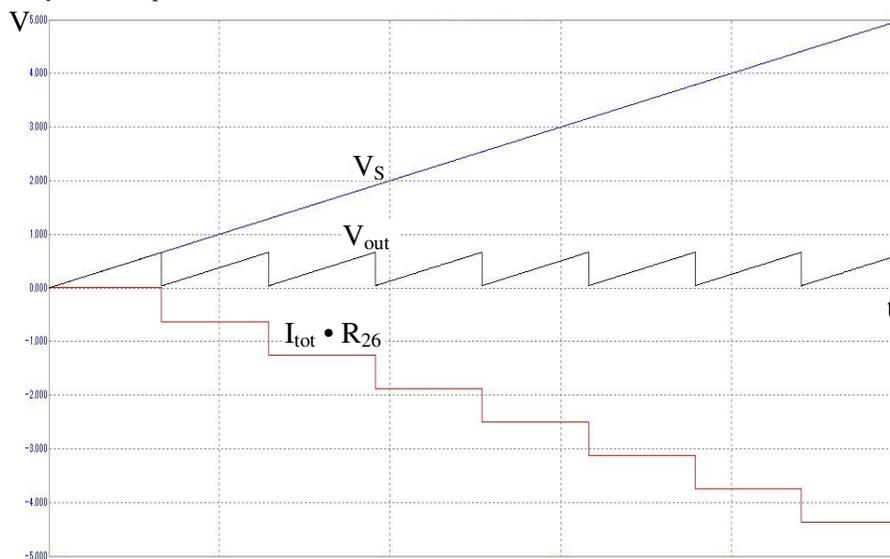


Figure. 8: Principal voltage waveforms that acts inside the circuit and the wanted V_{out} characterized by the typical saw-tooth waveform.

III. The experimental results

The circuit has been realized with discrete components. Both for NMOS and PMOS, we used very common and cheap components as ZVN2106 and ZVP4424 with the body connected with the source, and typical $V_{GS(th)}$ respectively equal to 1.8 V for the NMOS and -1.4 V for the PMOS. As operational amplifiers we used two LMC6482-AIN. The first is used for the buffer and the subtractor, the other for the inverting amplifier and the output adder. It is easy to individuate the seven NMOS-PMOS couples and the 10 and 100 k Ω resistors. The potentiometers are used to fix the voltage reference for each transistors couple and are supplied to 0 and -5 V. The first potentiometer fixes the negative offset voltage.

Figure. 9 shows the measurement bench with a stabilized energy supplier, a Philips PM3070 oscilloscope and a Yokogawa FG120 function generator and the realized circuit. The Yokogawa generates the input ramp, while the oscilloscope allows to monitor the output that correspond to the desired quantization error voltage.

In this phase of the circuit development, it is difficult to talk about its performances because, it is not yet optimized. With a resolution of three bits for the channels, with this kind of commercial MOSFETS, the time response at the last quantum is 7 μ s, while the uncertainty in the quantum discrimination that points out the ability to correctly recognize the quantum voltage, is equal to ± 8 mV.

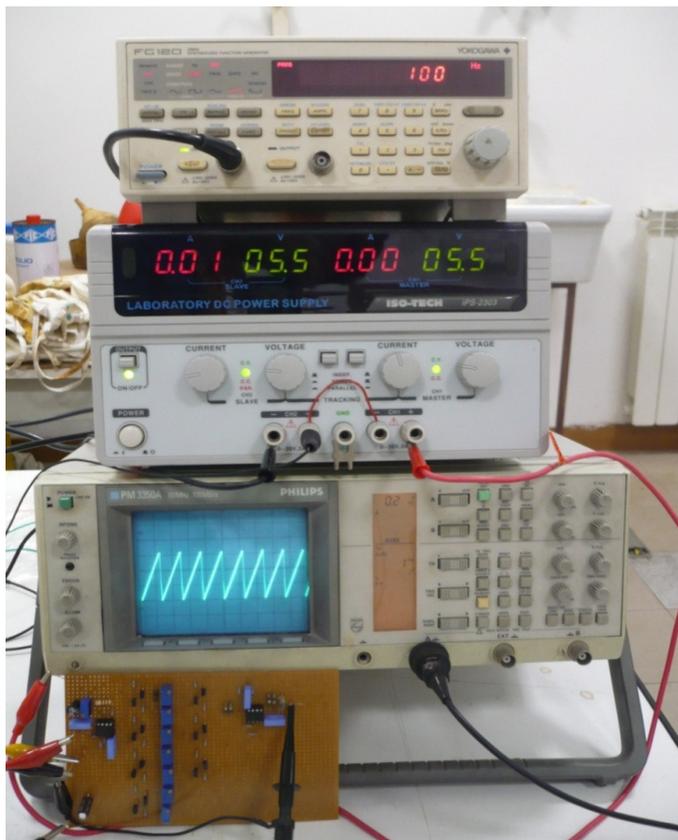


Figure. 9: Measurement Bench.

III. Conclusions

This is an “in itinere” work so to talk about conclusions can seem premature. We surely described a new kind of analog preprocessing circuit for linear folding ADC underlining the simplicity of the scheme. All the channels are similar and does not use components difficult to find on the market, for the case of discrete circuit, or difficult to realize in case of integrate development. The consumption of this apparatus is very low, implementing only two MOSFETS for channel. The circuit, after a wide simulation, has been realized by discrete components and tested. The next step will be to realize an integrated circuit of the proposed A/D to optimize the MOSFETS performances, to evaluate some characteristics as bandwidth or typical conversion errors, specific for this architecture, and to improve the resolution of this structure.

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