# Time-to-Digital Converter (TDC) with Sub-ps-Level Resolution using Current DAC and Digitally Controllable Load Capacitor

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***Abstract*—**This paper describes a cyclic time domain successive approximation (CTDSA) architecture that can be used as an interpolator in a time-to-digital converter (TDC). The new architecture of the CTDSA achieves adjustable sub-ps-level resolution with high linearity in ns-level dynamic range. The propagation delay adjustment is implemented by digitally controlling both the unit load capacitors and the discharge current of the load capacitance using current DAC. The proposed CTDSA achieves 610 fs resolution and ~2.5 ns dynamic range. The total simulated power consumption is 25.8mW with 5 MHz conversion rate with 3 V supply. The design was simulated using a 0.35 µm CMOS process.

## I. INTRODUCTION

Especially when using deep sub-micron technologies the signal processing is moving into time domain because the reduced voltage headroom makes it difficult to implement analogue signal processing functions. Furthermore, with deep sub-micron CMOS technologies the time domain resolution of digital signals is better than the voltage resolution of analogue signals [1]. In this work a cyclic time domain successive approximation converter (CTDSA) is designed to be used as a building block of a time-to-digital converter (TDC) architecture [2].

Reaching ps-level resolution in time-to-digital conversion is feasible for example with architectures that utilize the delay difference between the logic gates [3], the RC delay of the on-chip wiring [4], the frequency difference between two oscillators [5], time amplification [6], pulse shrinking [7], the difference between logic thresholds [8], passive on chip voltage divider [9] or random variation of the timing of the digital logic gates [10], [11]. In addition, multi-stage interpolation architectures have been developed to shorten the dynamic range and to improve the linearity of the interpolators providing the ps-level resolution [12].

In this paper, the high timing resolution of the CTDSA is achieved by digitally adjusting the load capacitance of a delay cell and by digitally controlling the discharge current of the load capacitance using a current DAC. Compared to the earlier design with an 8-bit DTC used in a TDC prototype [2], the 12-bit CTDSA architecture presented in this paper aims to improve the resolution, dynamic range and linearity of the TDC to make it possible to improve the single-shot precision, i.e. random error, to simplify the TDC architecture, to reduce the power consumption of the TDC, and to minimize the chip area. The paper is organized as follows. Section II explains the architecture of the TDC. In Section III design details and simulation results of the TDC are presented. The conclusions are summarized in Section IV.

## II. TDC

### A. Time Domain Successive Approximation

Successive approximation is a well-known principle used in the analogue-to-digital converters (ADC) to reach high resolution at the cost of conversion time. Successive approximation in time domain has been proposed on conceptual level, but not implemented for TDCs [13], and realized for clock de-skewing [14]. In this work the fine interpolation of a TDC is performed with a cyclic time domain successive approximation (CTDSA) method that resolves the time difference between two nonrepetitive signals one bit at a time in N cycles using binary search, as opposed to the previous, slower cyclic principles resolving the result LSB by LSB in $2^N$ cycles [15], where N is the number of bits in the conversion result.

### B. CTDSA Architecture

The key functional blocks of the CTDSA architecture of Fig. 1 are the digital-to-time converter (DTC) for binary controlled delay adjustments, phase detector (PD) for decision making, and shift register (SREG8) for storing the conversion result, which are analogous to the digital-to-analogue converter (DAC), comparator and successive approximation register (SAR), respectively, of ADCs based on successive approximation. The multiplexers, monostables and DTCs form two loops, highlighted in Fig. 1, in which the two signals representing the residue propagate during the cyclic conversion process [2].

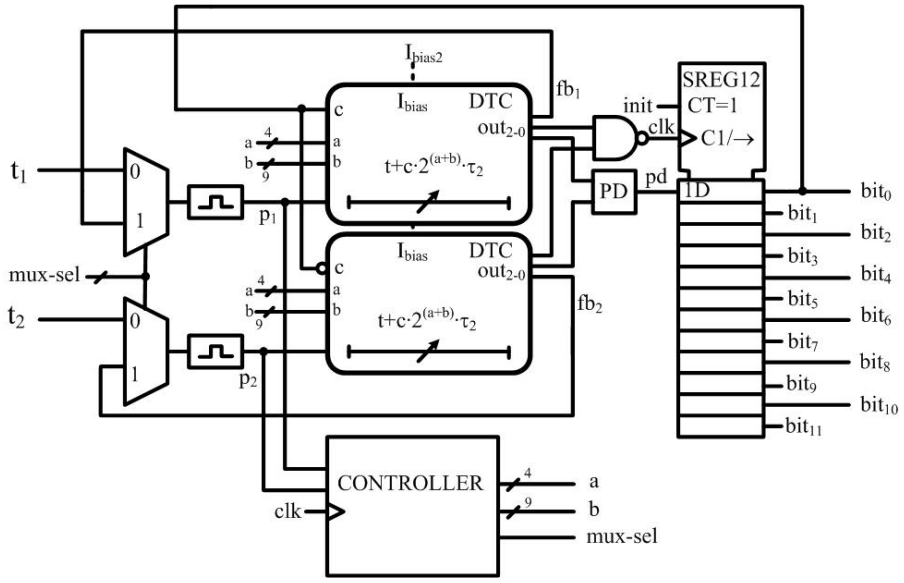


Figure 1. Block Diagram of CTDSA

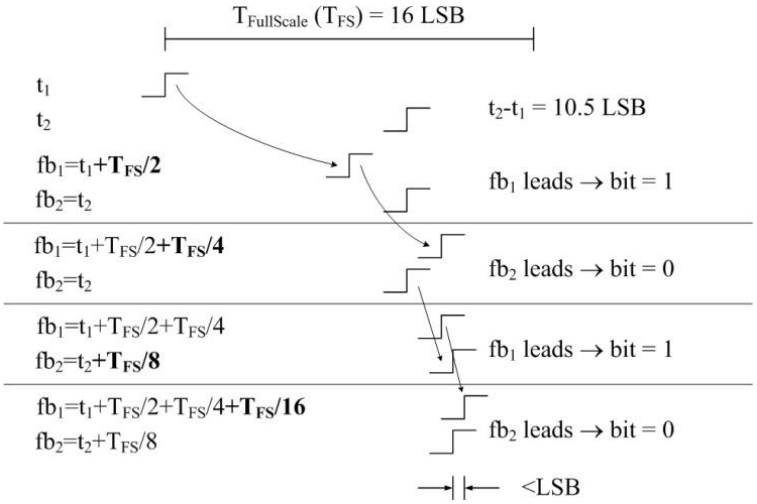


Figure 2. Operating principle of a 4-bit CTDSA method as a timing diagram [2].

### C. Operating Principle

The conceptual timing diagram of a 4-bit CTDSA is illustrated in Fig. 2, and Fig. 1 presents the realization of a 12-bit CTDSA. The CTDSA circuit resolves the time difference between two timing signals $t_1$, and $t_2$, in Figs. 1 and 2, triggering two loops in which feedback pulses, $fb_1$, and $fb_2$ in Fig. 2, propagate and their phases are adjusted until the time difference is resolved with the desired resolution. The bidirectional adjustment required by the binary search is implemented by making both signal paths adjustable, rather than keeping the propagation delay of one signal constant and adjusting the other one back and forth [2].

### D. TDC with Large Linear Dynamic Range and Sub-ps-Level Resolution

The CTDSA could be used as an interpolator in a TDC with large linear range provided for by a counter, as shown in Fig. 3. Each channel consists of a CTDSA for each timing signal (i.e. start and stop). The operating principle as a conceptual timing diagram is illustrated in Fig. 4. The measurement result, i.e. the time interval between the start and stop signals is obtained by combining the results of the counter (CTR) and the interpolators. The counter gives the number of full clock cycles between the start and stop signals, multiplied by the number of LSBs within the clock cycle. As shown in Fig. 4, the START and STOP signals are synchronized with the REFCLK by D-flip flops. The time difference, the residue, between $t_{11}$ (asynchronous) and $t_{12}$ (synchronous) and between $t_{21}$ and $t_{22}$ are measured by the CTDSA in each channel. Using the synchronous signals of the START and STOP a counter-enable signal is generated by AND gate to control the counter providing for large dynamic range.

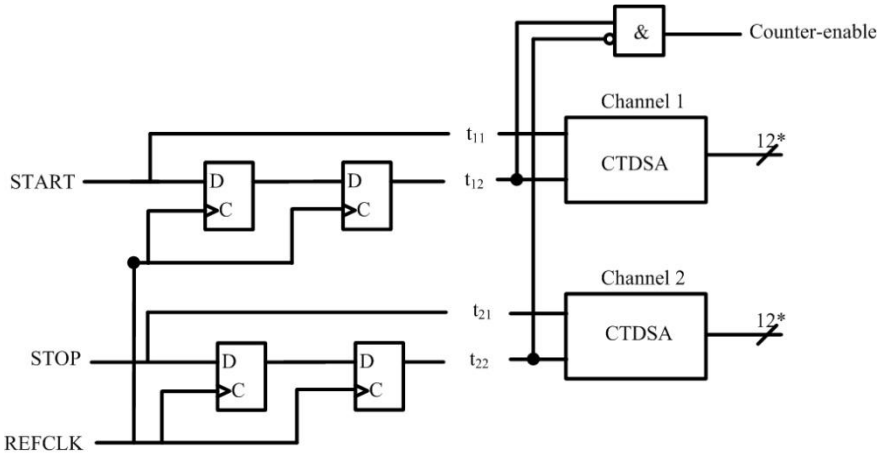


Figure 3. TDC with ns-level DR & sub-ps-level resolution

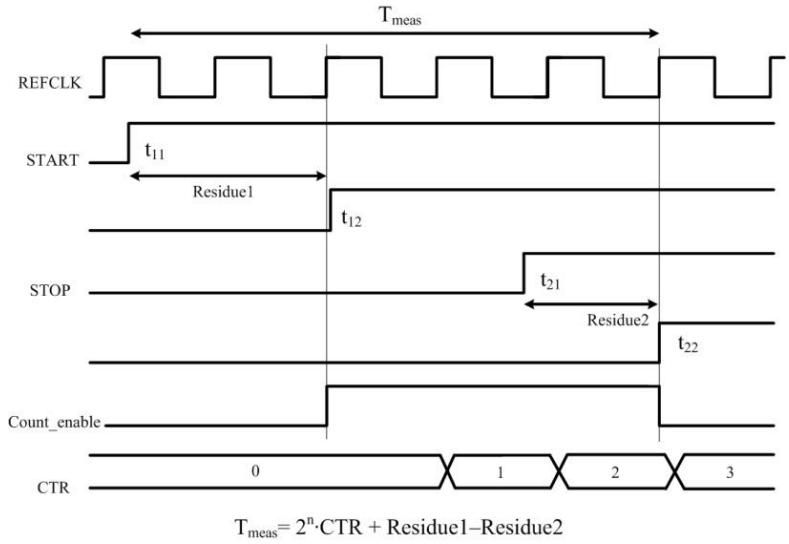


Figure 4. Operating principle of the TDC as a conceptual timing diagram.

**E. DTC Architecture**

The new DTC uses a current DAC with enable inputs a[3:0], a matrix of 256 digitally controllable moscaps as load capacitances, adjustable as blocks of powers of two with control signals b[8:0], and a comparator, as shown in Fig. 5. Depending on the control signals a[3:0] the discharge current of the load capacitance using current DAC can have four values $I_{bias}$, $2I_{bias}$,$4I_{bias}$, and $8I_{bias}$. With the control signals b[8:0] the apparent capacitance of the adjustable moscaps can be varied between two values depending on the value of the control signal CTRL of each block. Depending on the control signals of the digital loop filter D[9:0], $I_{bias}$ is obtained by the Current DAC_bias from the external current source $I_{external}$. The controlled $I_{bias}$ adjusts the dynamic range and resolution of the TDC. The DTC has three buffered outputs to isolate the two DTCs from each other.

Depending on the digitally controllable combination of the current DAC, $I_{bias}$, and the load capacitance the propagation delay of the DTC can be linearly scaled with 12 bits with a nominal resolution of 610 fs and 1.25 ns dynamic range. The new configuration makes it also suitable for high resolution clock de-skewing for example. In the binary search algorithm of the CTDSA method, however, only adjustments made as powers of two are required [2].

The main difference in contrast of the proposed design to the old DTC design used in [2], is the comparator in the output of the DTC block. The previous DTC [2] used a simple CMOS inverter as a comparator to determine when the capacitively loaded node CL was discharged below the inverter threshold value, as shown in Fig. 6. However, the slew rate dependency of the delay of the simple inverter limits the achievable linear dynamic range. The comparator has a much more stable propagation delay as a function of the input signal slew rate [16]. Using the comparator with the other input connected to the reference voltage Vref we can reach a much larger linear dynamic range in propagation delay scaling.

Compared to the design in [17], the biasing voltage is replaced with biasing current $I_{bias}$ as shown in Fig. 5. The biasing current $I_{bias}$ is scaled using current DAC to obtain the discharge currents of the load capacitance instead of the selectable delay cells.

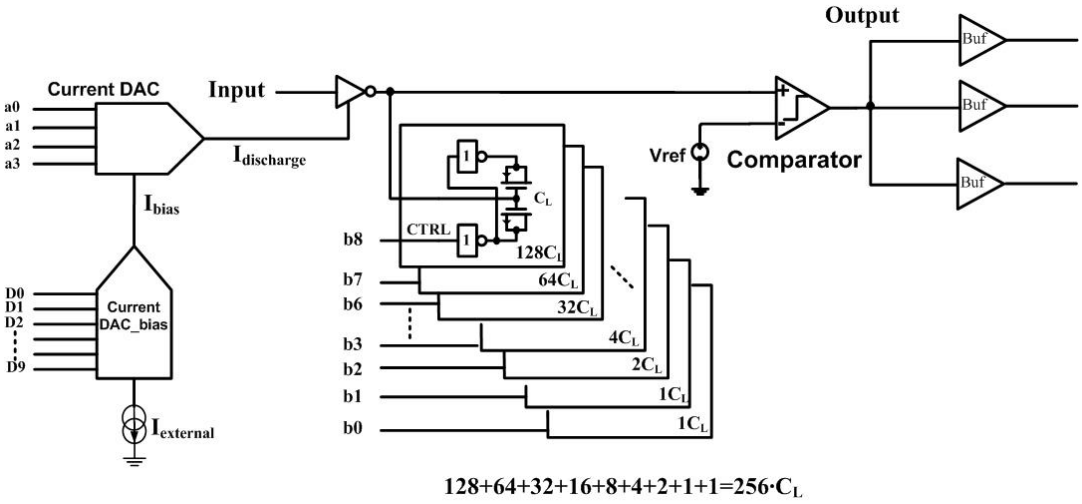


Figure 5. 12 bit Digital-to-time converter (DTC).

Improving the linearity by using a comparator and the current DAC allows for increasing the dynamic range. The resolution is increased by either increasing the resolution of the current DAC or the unit capacitor load. The new TDC achieves 12 bit linear dynamic range with the same number of the load capacitors compared to the previous 8 bit design [2].

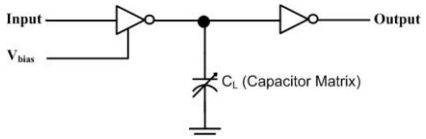


Figure 6. Previous Digital-to-time converter (DTC)

## III. CIRCUIT IMPLEMENTATION & SIMULATION

The design was simulated using 0.35 µm CMOS technology parameters while operating from 3 V supply.

### A. Current DAC

A Current DAC is used to adjust the delay cell in order to discharge the capacitor load. $I_{discharge}$ is used to adjust the delay cell. The current DAC is a simple binary weighted current mirror to reduce mismatch as shown in Fig.7. The current output of the DAC $I_{bias\text{-}output}$ is mirrored by PMOS and NMOS current mirror M5-M8. Transistors M5-M8 are sized so as to give enough swing for the DAC. The current mirrors are connected to NMOS switches. $I_{bias}$ is obtained by 10 bit Current DAC_bias from $I_{external}$. The simulated power consumption of the DAC is less than 19.8 mW at nominal operating point, $I_{bias}$=410 uA.

$I_{bias}$ is digitally controlled by digital loop filter to adjust the dynamic range and resolution of the TDC. The operating point is locked to the cycle time of the reference clock using a DLL [2]. The dynamic range of the TDC is set by the reference clock. The Current DAC_bias makes it possible to adopt the propagation delay to the given application and giving conditions so that the propagation delay can be stabilized against the process, voltage and temperature variations. Current DAC_bias is implemented by current mirror like the Current DAC in Fig.7.

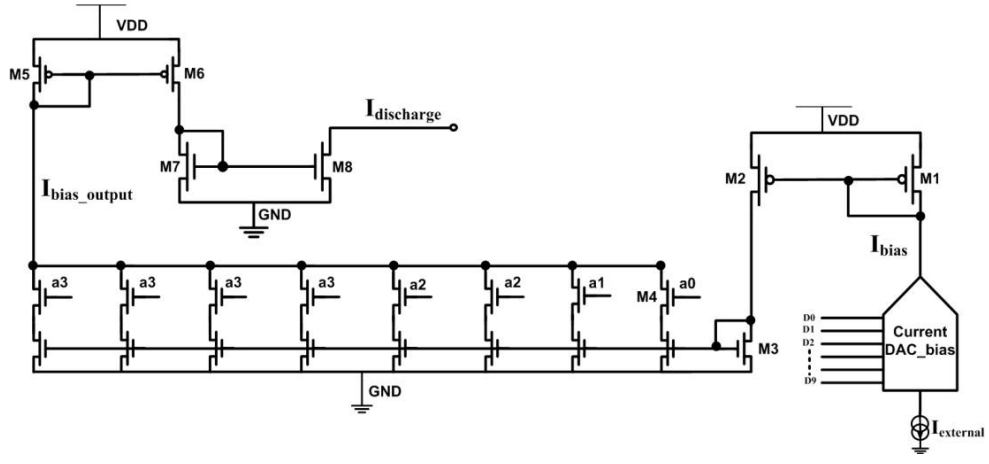


Figure 7. Current DAC

### B. Adjustable Delay Cell

The schematic of the delay cell is shown in Fig. 8. The delay cell is a current starved inverter. The overall propagation delay of the delay cell can be adjusted with a scaled bias current $I_{bias}$, Instead of using selectable delay cells and only scaling the load capacitance, which markedly reduces the layout area compared to [2], [17] with the same dynamic range and resolution.

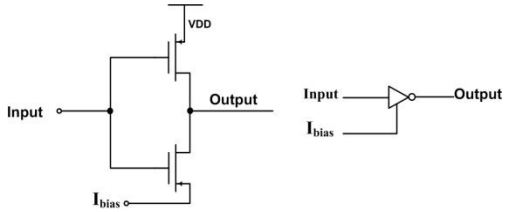


Figure 8. Schematic of Adjustable and Selectable Delay Cell

### C. Comparator

The schematic of the two stage comparator is shown in Fig. 9. The output stage is a current sink/source inverter [18]. M6 was sized to have sufficient current to reduce the slew rate [18]. To make sure that the comparator has constant delay regardless of the input signal slew rate, the bandwidth has to be large [19]. Therefore, $I_{bias\text{-}comp}$ was chosen to have large bandwidth without significantly increasing the power consumption of the whole DTC [16] [18]. The simulated static power consumption of the comparator is less than 1.1 mW.

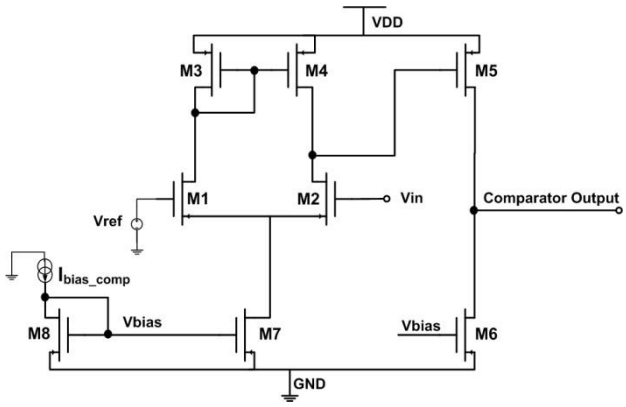


Figure 9. Schematic of the Comparator

### D. TDC Simulation

A 625 ps delay difference between asynchronous and synchronous signals is applied to the CTDSA. Fig. 10 illustrates the operation of the CTDSA to measure the residue. The CTDSA is successful to converge the final residue within an LSB.

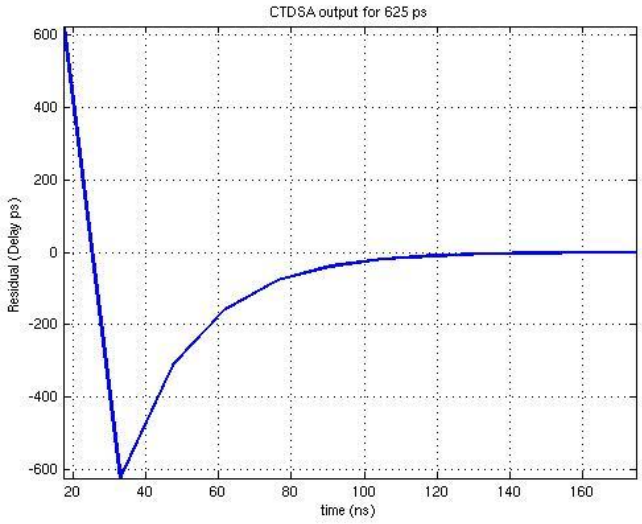


Figure 10. Operation of CTDSA

The TDC is simulated for five different time intervals (0, 625, 1250 1875 2500) ps. The corresponding digital word to the delays is presented in Fig, 11. The digital output for the five delays corresponds to the theoretical output. Multiplying the digital output with LSB (610 fs) equals to the time interval. For example, 4095*610fs~2.5ns.

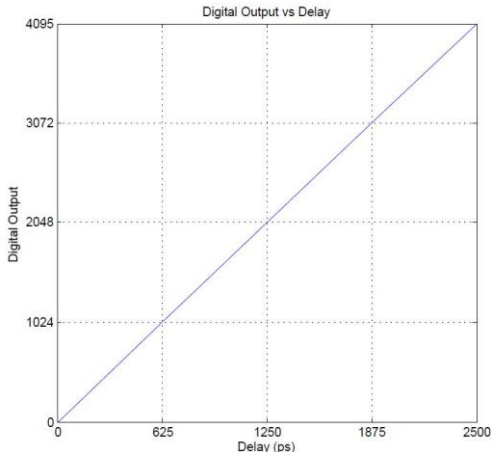


Figure 11. New CTDSA

## IV. CONCLUSIONS

In this paper, a 12-bit cyclic time domain successive approximation Time-to-Digital Converter using a comparator instead of a simple inverter and current DAC instead selectable delay cells improves the linearity of the DTC. Combined with a counter sub-ps resolution and ns-level dynamic range feasible for a general purpose TDC. However, to limit the size of the capacitor matrix, current DAC is used to scale the capacitor discharge current. The CTDSA was verified with different delays within the dynamic range. The digital outputs correspond to the theoretical output. The total simulated power consumption is 4.23 mW with 5 MHz conversion rate and 3 V voltage supply.

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