2011 International Workshop on ADC Modelling, Testing and Data Converter Analysis and Design and IEEE 2011 ADC Forum
June 30 - July 1, 2011. Orvieto, Italy.

A Flash Time-to-Digital Converter with Two Independent Time Coding Lines

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Abstract-We present a time-to-digital converter with a virtual time coding line created as an equivalent of two independent time coding lines operating simultaneously. Proposed solution allows to overcome the technology limitation in achievable resolution and improve the precision of conversion. The new coding line used in the interpolating time counter designed in an FPGA CMOS device provides the precision (standard deviation) below 35 ps within a 1 s measurement range.

I. Introduction

Various methods in the analog and digital domain have been developed for precise time-to-digital conversion [1]. At present the most popular conversion technique is based on the use of the Nutt interpolation method [2] and a single time coding line (TCL) in the form of a tapped delay line in each interpolator. The advantage of this technique is simple realization in digital integrated circuit and short conversion time. However, the achievable resolution of conversion is limited by the propagation time of the fastest delay element used to create the TCL. It directly depends on the microelectronic technology utilized for the circuit fabrication and the natural way to improve the resolution is choosing a faster technology. Another way to improve the resolution is the use of two identical TCLs shifted one to another by half of unit delay (TCL resolution) [3, 4]. Since in FPGA devices we cannot introduce very short delays (tens of picoseconds) of precisely controlled value, that method may be used only if the expected resolution is at the level of hundreds of picoseconds [5]. We propose the use of two TCLs operating independently, whose transfer functions are used to create a single equivalent transfer function. The main advantages of this approach are: (1) the resolution is improved approximately twice compared to single TCL, and (2) the time offset between the lines is not significant and has not to be controlled in design.

II. Equivalent Coding Line

A. Method

To create a virtual equivalent coding line (ECL) the transfer functions of both TCLs used (TCL1 and TCL2) have to be identified. It is usually made with the aid of the statistical code density test (SCDT) [6], by precise identification of the quantization steps (m and n) of each TCL within a single period T_o of the reference clock (fig. 1).

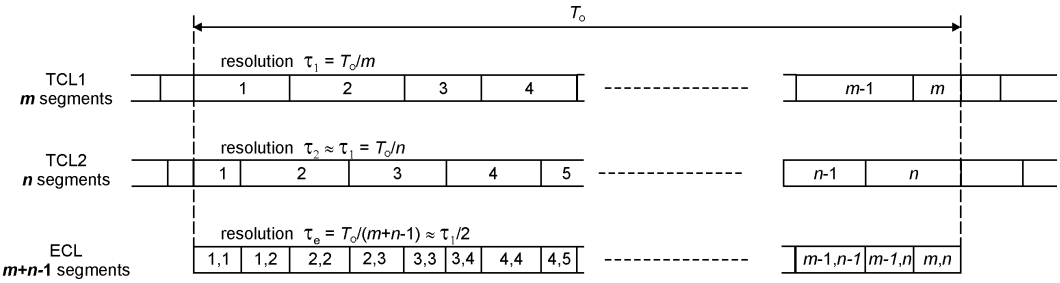

Figure 1. Creation of the equivalent coding line

If we denote the consecutive quantization steps of the first TCL as $QS1_i$ ($0 < i \leq m$), and of the second TCL as $QS2_j$ ($0 < j \leq n$), the ECL is divided in the quantization steps QSE_{ij}. Each step begins at $QSEb_{ij}$

$$QSEb_{ij} = p\sum_{k=1}^{i-1} QS1_k + (1-p)\sum_{k=1}^{j-1} QS2_k \quad (1)$$

where p is a predicate

$$p = \left(\sum_{k=1}^{i-1} QS1_k \geq \sum_{k=1}^{j-1} QS2_k\right)$$

and ends at $QSEe_{ij}$

$$QSEe_{ij} = p\sum_{k=1}^{i} QS1_k + (1-p)\sum_{k=1}^{j} QS2_k \quad (2)$$

where

$$p = \left(\sum_{k=1}^{i} QS1_k \leq \sum_{k=1}^{j} QS2_k\right)$$

The duration of the ij-th quantization step is

$$QSE_{ij} = QSEe_{ij} - QSEb_{ij} \quad (3)$$

When the coding lines TCL1 and TCL2 contain respectively m and n time quantization steps, their mean resolutions are $\tau_1 = T_o/m$ and $\tau_2 = T_o/n$. Since both lines are located close each other on the same silicon chip, they have similar parameters: $m \approx n$ or $\tau_1 \approx \tau_2$. The ECL resolution is $\tau_e = T_o/(m + n - 1)$. Having in mind that for typical converters $m \approx n$ and $m >> 1$, the resulting resolution τ_e is approximately two times better compared to the resolution of a single TCL ($\tau_e \approx T_o/2m \approx \tau_1/2 \approx \tau_2/2$).

B. Hardware

The transfer function of each TCL is calculated and stored by the code processor shown in figure 2.

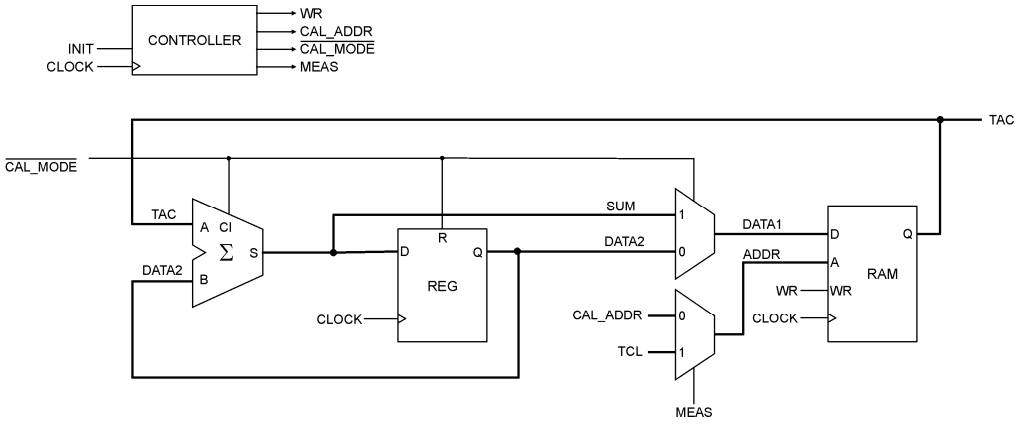

Figure 2. Code processor

To calculate the TCL transfer function two operations are performed consecutively: identification and processing. In the *identification phase* (CAL_MODE = 1, MEAS = 1) the density test (SCDT) is realized. The random time intervals are digitized by TCL and the coded output words (TCL) are used as addresses for the RAM memory. At a given address, the RAM output word TAC is first read (WR = 0), incremented by one in the adder (CI = 1) and saved as the input word DATA1 (WR = 1). This cycle is repeated to obtain a sample of reasonably large size. Then, in the *processing phase* (CAL_MODE = 0, MEAS = 0) the array containing the identified transfer function of the TCL is calculated. The controller increments the address CAL_ADDR and the register accumulates the sum of successively read memory words. The consecutive sums are written back into the RAM memory. The 10-bit output word (TAC) provides 10-bit resolution of the TCL transfer function. Thus for the clock period T_o = 4 ns we obtain a 4 ps resolution, which allows to identify the transfer function accurately.

The identified transfer functions of both TCLs may then be used to calculate the transfer function of the ECL using the merging formulas (1) and (2). However, such an approach results in significant consuming of the FPGA logic resources and area. Therefore we introduced an improved solution based on dynamic calculation of the ECL quantization step for each measurement. During the measurement (MEAS = 1, WR = 0) the TCL output data (TCL) is used as the RAM address to read the time coding result (TAC, fig. 2). The output words TAC1 and

TAC2 of code processors related to both TCLs are then used to calculate the related ECL quantization step and the result of conversion. Figure 3 presents the calculation procedure.

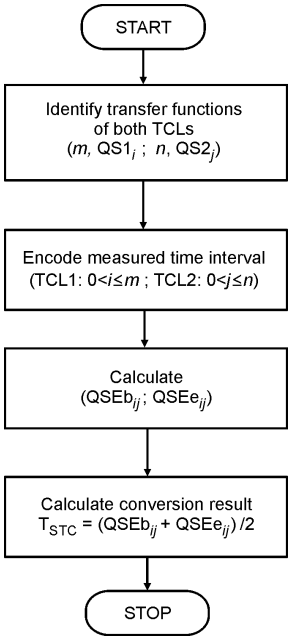

Figure 3. Calculation of the conversion result

III. Design of time interval counter

We designed a time counter based on the two-stage interpolation with the ECL in each interpolator (fig. 4). The first interpolation stage (FIS) allows for detection and registration of the four-phase clock (FPC) segment in which an input pulse (START or STOP) appears. In the second interpolation stage (SIS) for precise time-to- digital

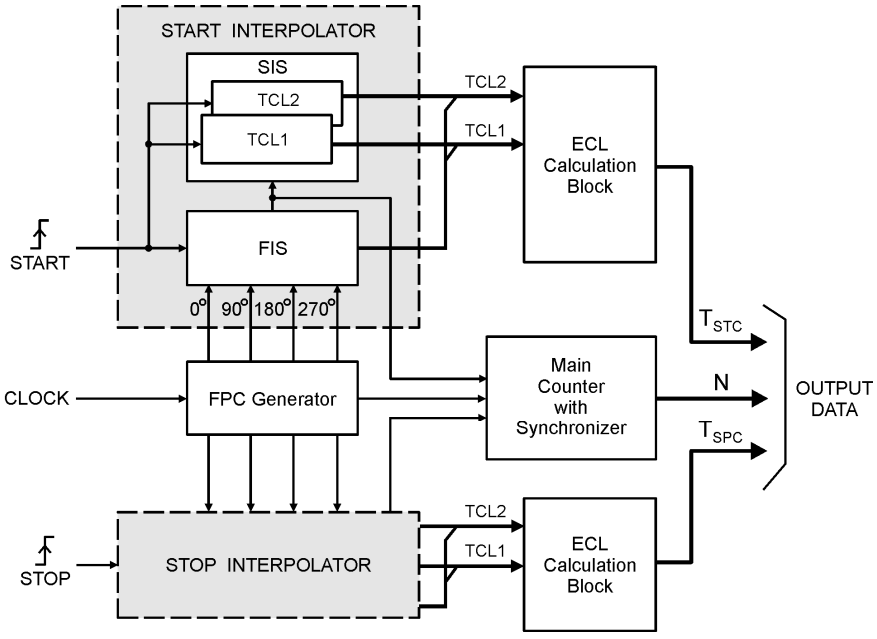

Figure 4. Simplified block diagram of the time counter with two TCLs in each interpolator

conversion within a single phase segment of the FPC we used two TCLs created as delay lines consisting of non-inverting buffers and D flip-flops [7]. As buffers we utilized the multiplexers forming the fast carry chains in the FPGA device. The delay time of such a multiplexer is about 45 ps and this is the time resolution of each TCL. The raw data from the FIS and SIS represented respectively in one-cold and thermometrical codes are then converted into natural binary code. These data are used as a RAM addresses in the code processors operating in the measurement mode.

The wide measurement range in the Nutt interpolation technique is achieved by counting the periods T_o of the reference clock. We utilized a 40-bit serial counter and a 250 MHz clock to obtain the measurement range of about 73 minutes. Since the frequency of the clock is relatively high and the start and end of the measured time interval are asynchronous with respect to the clock, the counter must be carefully synchronized. Otherwise, the counting process would be affected by the metastability effect that would deteriorate the precision of time interval measurement. A dual-edge double synchronizer [7, 8] has been utilized in this design. For higher clock frequencies the auto-tuned synchronization principle was also successfully tested [9]. Since the output data T_{STC} and T_{SPC} are normalized to T_o, the measurement result is simply calculated as $T = (N + T_{STC} - T_{SPC})\, T_o$, where N is the decimal equivalent of the binary content of the main counter.

The integrated time counter has been used in a portable time counter module which may be controlled by any (net)notebook via the USB interface (fig. 5) [10]. The module has the dimensions 140 mm x 70 mm x 17 mm and is supplied from a single USB 2.0 interface.

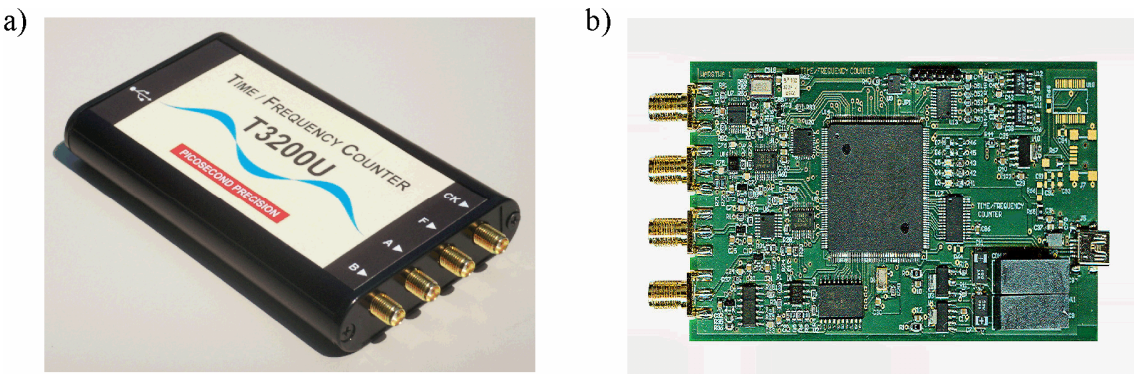

Figure 5. Time counter module (a) and its internal view (b)

III. Test results

The first test of the time counter module was performed at a room temperature of about 20 °C and with nominal supply voltages. Figure 6 shows the integral linearity characteristic of the START interpolator obtained with the use of the SCDT performed with a large sample size ($2^{18} - 1$). The characteristic contains 169 channels covering the single clock period (4 ns). Hence the mean value of the resolution (bin width) is about 24 ps (1 LSB). When a single TCL was used in the same interpolator the characteristic consisted of 89 channels and the resolution was 45 ps or twofold worse [7].

The high effectiveness of the presented time coding principle manifests itself also in significant improvement of the conversion linearity. The worst-case value of the integral linearity error for a single TCL was 94.5 ps and was lowered to 55.7 ps for the ECL (fig.6). The performance of the STOP interpolator is similar.

The precision of the time counter module was estimated as the standard deviation calculated from the samples of time intervals varied from 10 ns up to 1 s (fig. 7). The precision below 35 ps rms was obtained within the range up to 200 ms when the on-board TCXO was used as the reference clock, or within the whole measurement range when using an external atomic standard. When the counter was programmed to utilize only a single TCL in each interpolator, the resulting precision changed to 70 ps rms.

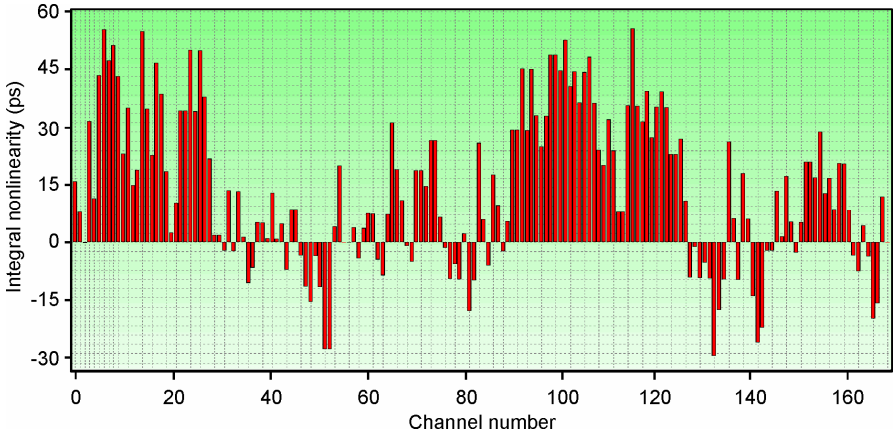

Figure 6. Integral nonlinearity of the START interpolator with ECL

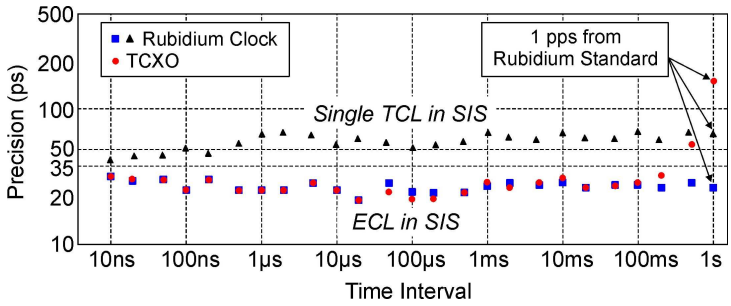

Figure 7. Precision of the interpolation counter with a single TCL or an ECL in each interpolator

The described counter device has been utilized to design three counter instruments: the mentioned portable time counter module with USB interface, the computer board with PCI interface, and the wireless module with WiFi interface [11]. The instruments allow to measure time intervals with the precision better than 35 ps and the maximum measurement rate reaching 5×10^6 measurements per second. The additional measurement modes include the frequency measurement (up to 3.5 GHz), frequency sampling (up to 2 MSa/s), calculation of Allan Deviation, Time Interval Error (TIE, MTIE), and Time Deviation (TDEV).

IV. Conclusion

The presented principle of time coding with ECL has three main advantages as compared to the single TCL coding: (1) twofold improving of the resolution and precision of the TDCs for a given microelectronic technology, (2) simple design of the independent time coding lines, and (3) not extended conversion time. The principle may further be expanded to create ECL with more than two TCLs.

References

[1] J. Kalisz, "Review of methods for time interval measurements with picosecond resolution", *Metrologia*, vol. 41, pp. 35–51, 2004.
[2] R. Nutt, "Digital time intervals meter", *Rev. Sci. Instrum.*, vol. 39, pp. 1342–1345, 1968.
[3] G. Braun, H. Fischer, J. Franz, A. Grunemaier, F. H. Heinsius, L. Henning, K. Konigsmann, M. Niebuhr, M. Schierloh, T. Schmidt, H. Schmitt, H. J. Urban, "*F1 – An eight channel time-to-digital converter chip for high rate experiments*", Proc. 5th Workshop on Electronics for LHC Experiments, Snowmass, 1999.
[4] "*TDC-GPX. Ultra-high performance 8 channel time-to-digital converter*", Datasheet, Acam, 2006.
[5] M. Zieliński, D. Chaberski, S. Grzelak, "*Time-interval measuring modules with a short deadtime*", Metrology and Measurement Systems, vol. X, no. 3, pp. 241–251, 2003.

[6] J. Kalisz, M. Pawłowski, R. Pełka, "*Error analysis and design of the Nutt time-interval digitiser with picosecond resolution*", J. Phys. E, Sci. Instrum., vol. 20, no. 11, pp. 1330–1341, 1987.
[7] R. Szplet, J. Kalisz, Z. Jachna, "*A 45 ps time digitizer with two-phase clock and dual-edge two-stage interpolation in Field Programmable Gate Array device*", Measurement Science and Technology, vol. 20, 025108, 11 pp., 2009.
[8] A. Mäntyniemi, T. Rahkonen, J. Kostamovaara, "*A 9-Channel integrated time-to-digital converter with sub-nanosecond resolution*", Midwest Symp. Circuits and Systems MWSCAS'97, vol. 1, pp. 189–192, 1997.
[9] R. Szplet, "*Auto-tuned counter synchronization in FPGA-based interpolation time digitizers*", Electronics Letters, vol. 45, no. 13, 2009
[10] R. Szplet, Z. Jachna, K. Rozyc, J. Kalisz, "*High precision time and frequency counter for mobile application*", WSEAS Transactions on Circuits and Systems 9 (6), pp. 399-409, 2010
[11] www.vigo.com.pl