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Wideband two-phase generator for testing multiple ADCs in measurement systems

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Abstract - A two-phase generator board has been investigated as a mean to perform precision tests on the ADCs of measurement system for wideband distorted power measurement. To overcome the limitation of the commercial generator in the lower frequency band, a design modification has been introduced. Verification of the characteristics of the generator shows the possibility of operation for in the low frequency range and the a phase shift is contained within 10 mrad up to 2 MHz. A characterization in terms of spectral purity and voltage stability of single tone synthesized are reported.

I. Introduction

The present work aims at the development of a two-phase generator, able to generate suitable synchronized waveforms at both outputs for characterizing measurement systems of precision analog to digital converters (ADCs) for sampling the signals, for example those that are employed for the determination of the power or the power quality parameters. In fact, the characterization of multiple ADCs systems employed for sampling those waveforms is necessary, especially for evaluating the corrective factors in the determination of the total power or of the power associated to the harmonic components. Another use of the information derived by this characterization can be applied to the evaluation of the uncertainties, as for example in [1].
The generator is built around a commercial board [2] with high speed and high resolution. In principle, for its high resolution DACs, the board can be employed also for supplying signals calibrated in amplitude. However, this system is mainly employed for its high sampling rate, which, besides its high resolution, allow us to program the signals with a sharp time definition and, consequently, a good phase definition of the different harmonic components of the waveform.
Different test functions are being implemented with this generator, as for example:

- Sinusoidal signals with programmed characteristics at the two outputs. These sinusoidal signals with programmed amplitude and phase will be mainly used to verify the relative delay between different channels in an acquisition system.
- Multitone signal generation at the same output. The aim of this operational mode of operation is the investigation of the linearity of the phase shift in a single channels.
- Signals with a programmed time jitter or phase shift variations for the dynamic verification of the acquisition time characteristics.
- Generation of specific pulse signals for other purposes.

II. The generator

A. Characteristics of the generator selected

The generator is based on an open platform commercial board. There are two main blocks: a high performance FPGA board and an auxiliary board based on a double channels digital to analog converter and a high frequency PLL.
The main features of the DAC employed in the system are a vertical 16 bit resolution and a speed update rate up to 1 Gsamples/s for each channel. Optimal performances are made when the high speed clock is provided from a voltage controller crystal oscillator (VCXO) that is controlled by means of a high performance PLL clock synchronizer, which accepts frequencies up to 2.2 GHz. The clock synchronizer for proper operation needs two reference clock inputs: the primary and the secondary. In our Institute the primary clock can be derived directly from the primary atomic clock distributed at the frequency of 10 MHz. The PLL synchronizer has an efficient jitter cleaning, low phase noise and several outputs that can be programmed independently in order to provide

several high performance clock signals. Two main clocks are generated with the PLL synchronizer one at the frequency of about 1 GHz, which controls the DACs' operation, and an intermediate frequency clock at about 250 MHz, which control the two DDS high performance devices implemented at the FPGA level.
For the time resolution, below 1 ns, the electromagnetic coupling between adjacent currents path is more critical. This is a key issues that limits the performance of ultra high speed electronics system based on silicon technology. More problems arise when we need to distribute high clock frequencies on multiple devices or when we need to synchronize with high precision several blocks of the same system at the same front of the clock. In this case jitter phenomena are crucial for the goodness of the system. FPGA architecture offers the advantage to make possible the design of high performance digital devices and to synchronize them accurately, by using distribute clock architecture, which optimizes the path of clock signals to reduce latency and power.

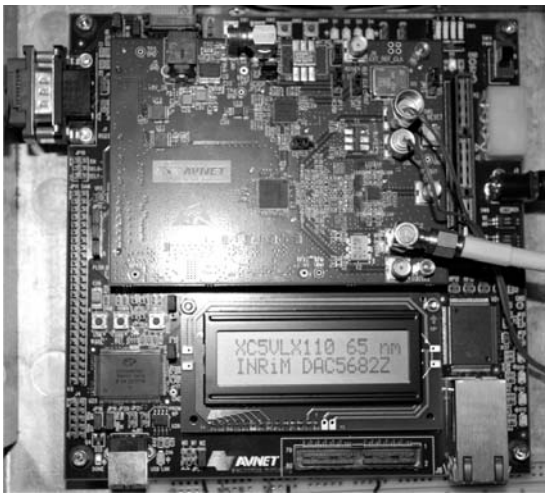

Figure 1. Photo of the generator, the high speed double output 1 Gsample/s DAC is mounted on a FPGA board based on Virtex5 device.

B. Modification of the commercial project

High speed digital to analog converters (DACs) have a complementary current output signal, thereby the current output signals are differential. This differential current signal is converted, typically, to a voltage signal with a current to voltage converter (CVC).
The high speed DAC under investigation has a double output structure. Each output is formed by an array of cascoded NMOS transistors as sink current and a series of switch array which under the control of the switch driver provide the connection of the appropriate current-source/sink to the outputs. So, the stack of the current source/sink and differential switches provide an output impedance of about 300 kΩ in parallel with an output capacitance of 5 pF.
The array of output transistors limits the minimum output compliance and beyond this value transistor breakdown may occur. Distortion performance and integral non linearity are sensible when the minimum compliance voltage is exceeded and the best performances in terms of distortion are achieved when the full scale signal at the output does not exceed 0.5 V. The maximum current capability of the DAC is about 20 mA for each channel.
Typically, high speed DACs used for RF applications are generally configured to drive 50 Ω double terminated properly selected RF transformer, which does not allows operation in dc and low frequencies. However, the high bandwidth input data bus of 1 Gsamples/s and the vertical resolution of 16 bits are suitable for a high speed precision arbitrary synthesizer for wideband signal generation, which can be used both in the acoustic and in the ultra acoustic band.
A wideband differential transimpedance stage, for current to voltage conversion, is implemented with a resistive network for dc coupled application or with a transformer for ac coupled application. Design which requires high precision and isolation to protect the DAC output as well as wideband working are based on differential transimpedance circuits realized with wideband dual operational amplifier or with fully differential operational (FDA). Fig. 2 shows a preliminary configuration of the output structure for high speed DAC which is composed by two key stages, a bias network and a high speed amplifier (HSA). The HSA is configured as a difference amplifier and performs a differential to single ended conversion buffering the output of the high speed DAC.

The bias network formed by resistors R_{b1}, R_{b2}, R_{b3}, R_{b4} should be calculated adequately, solving a set of current and impedance equations [2] in order to provide bias and impedance termination for the DAC output.
The resistors R_1=R_2=R_3=R_4 set the gain to unit for the HSA device.

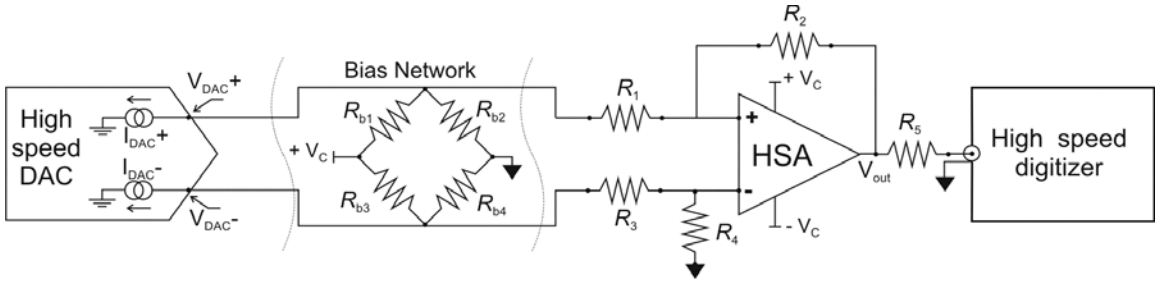

Figure 2. Output structure of a single channel of the high speed DAC.

The structure and the high frequency working of this device need particular consideration regarding the current path leakage as well as the substrate where the devices will be mounted.

C. Program for generating the signals

The software for the generation of the suitable signals has been written inside the FPGA which provides the control of internal register of the DAC as well as the two direct digital synthesis (DDS) devices. A user can use in simple and immediate way the hyperterminal application which ensures the full control of the device without writing programming code. However, it is possible to write suitable applications in any programming languages with the advantages that the user does not install any driver and can use a simple serial or serial to USB generic converter in order to communicate with the generator.

III. Preliminary characterization of the generator

A preliminary comparison in terms of working band between the two DACs' output. One of the channels is buffered by means a differential miniature electromagnetic transformer (factory configuration). The other one is modified and a HSA device having low noise, high slew rate, unity gain and bandwidth up to 1.8 GHz has been used. In the channel buffered with the HSA stage the phase shift between the output and the input, measured by a high speed 10-bit digitizing oscilloscope, resulted less than 10 mrad up to 2 MHz and less than 50 mrad up to 10 MHz. Hovewer, using HSA stage is possible to generate low frequencies ac signals as well as dc signals which are not permited if the autput of the high speed DAC is bufferd with differential wideband transformer.

A. Spectral measurements of single tone ac signals

The total harmonic distortion up to tenth harmonic of single tone sinusoidal signals generated by means of the high speed generator constructed has been measured by a signal analyser having bandwidth from 9 kHz to 1.5 GHz.
During the test several single tone sinusoidal signals have been synthesized. The amplitude of all signals was constant. In Fig. 3 the spectrum of a single tone of 1 MHz from 50 kHz to 20 MHz is shown. In this band external disturbances seems to be absent up to 90 MHz, but in all synthesized tones spectral lines near to 100 MHz appear. These disturbances probably arise from the clock of the soft core processor employed. Beyond this frequency the spectrum appears flat up to 1 GHz.
The harmonic distortion of the tones from 50 KHz up to 50 MHz has been measured by the same signal analyser, which permits to measure up to ten harmonics starting from the fundamental one. The results are reported in Fig. 4.
However, we checked at various tones the quantity spurious free dynamic range (SFDR), [4], which is defined as the amplitude difference between the fundamental and the largest harmonically or non-harmonically related spur from the dc to the full Nyquist bandwidth ($f_{Samplig\_Rate}/2 \cong 500$ MHz). This quantity is one of the main parameters included in the high performance DDS core, which is depends on the DAC resolution and the operating frequency of DDS core. In this design this parameters has been set to about 96 dB, with DDS system clock of 250 MHz and frequency resolution of 0.1 Hz.

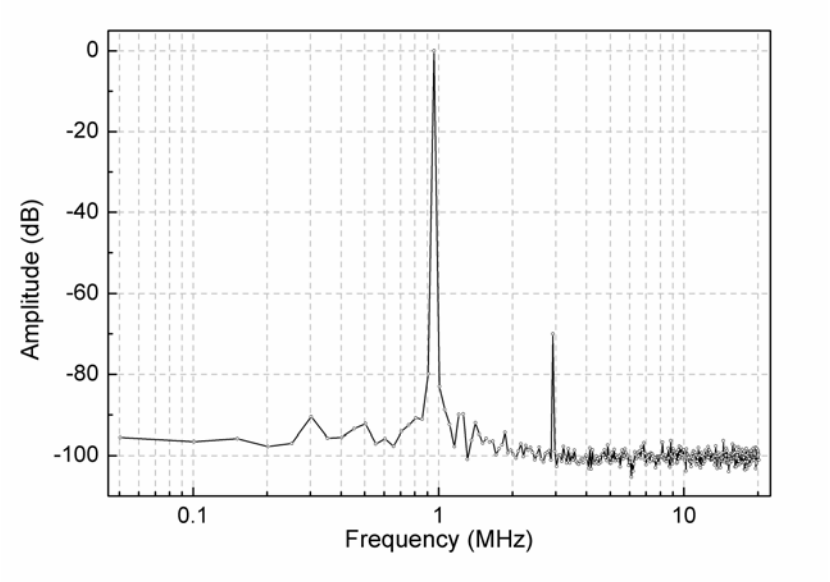

Figure 3. Spectrum of a single tone at 1 MHz.

In Tab. 1, is reported the quantity, total harmonic distortion, computed as:

$$\mathrm{THD} = \frac{\sqrt{\sum_{i=1}^{10} V_i^2}}{V_1} \qquad (1)$$

where, i, represents the harmonic measured with the signal analyser.

Frequency (MHz)	0.05	0.1	0.49	1.97	4.92	9.83	19.66	49.15
THD (%)	0.15	0.04	0.02	0.21	0.07	0.17	0.35	0.83

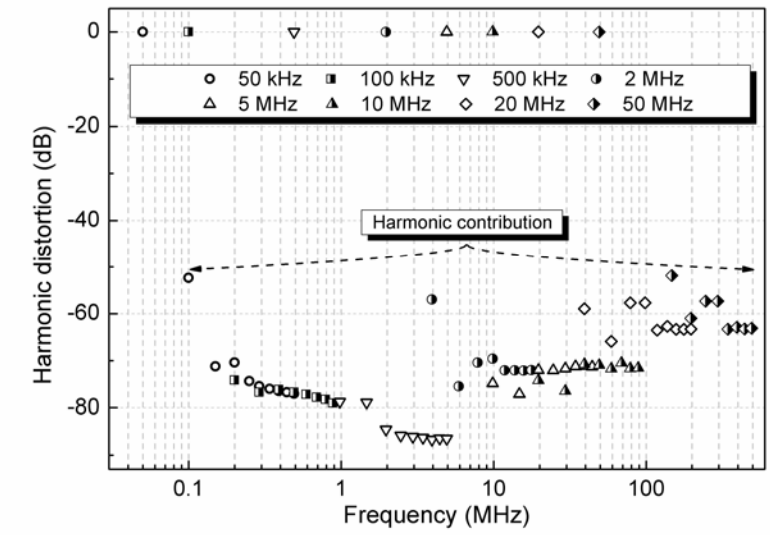

Figure 4. Harmonic contribution, up to ten, of ac single tones synthesized.

B. Voltage stability of the output DAC

The output voltage of the DAC has been monitored with a thermal voltage measuring instrument. Keeping constant the voltage level several tones have been synthesized from 20 Hz to 1 MHz. The voltage level has been chosen by setting the output current of the high speed DAC at about 16 mA. The current level can be set in according with $(V_C/R_{bias})\cdot(DAC_{Gain}+1)$, where DAC_{Gain} is an integer number between 1 to 16. This current, in the resistive bias network, generates a differential voltage which is then scaled by a differential amplifier with constant gain about 1. In Fig. 5 the amplitude relative error for frequencies from 40 Hz to 1 MHz is shown. All measurements are made with a coaxial cable with a length of 20 cm and two BNC connector. Type A uncertainty, at 1-σ level, is about 45 ppm up to 1 MHz. The expanded uncertainty (k=2) of the measuring system, a commercial thermal voltmeter, used to characterize the output of the high speed DAC is about 40 ppm up to 20 kHz; 300 ppm up to 500 kHz and 600 ppm at 1 MHz.
To characterize the voltage level up to 100 MHz a preliminary measuring system based on a high frequency single junction thermal converter is under construction. Single junction thermal converts have a simple input structure, so they can be used for the characterization of RF voltages. The low output electromotive force should be measured carefully in order to obtain the requested accuracy.
In the range from 1 MHz to 100 MHz e new class of multijunction thermal converters, [5], have been constructed having an ac/dc error less than 0.5 % at 100 MHz with the model having bifilar haters. Unfortunately, this MJTCs are not at the moment available commercially.

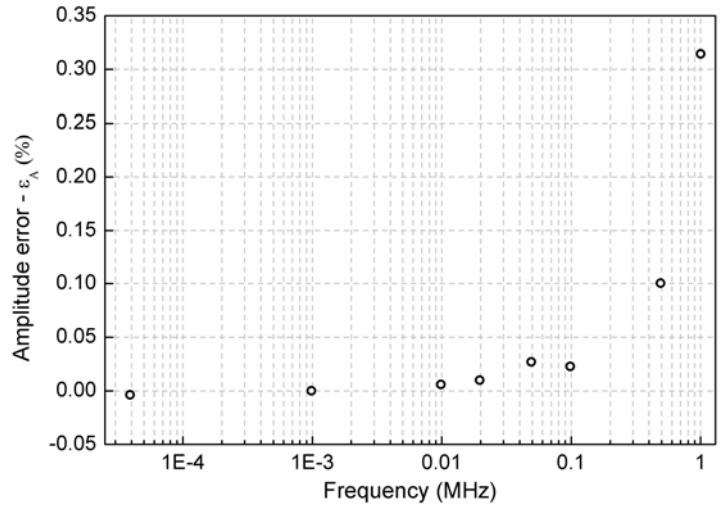

Figure 5. Amplitude relative error, respect to 1 kHz, at various frequencies.

IV. Conclusions

A double-phase generator for testing the frequency and phase characteristics of ADCs in measurement systems has been set up. The circuit of an available high resolution and high speed generator has been modified by introducing a differential transimpedance circuits realized with a wideband high speed operational amplifier. In this way the generator is able to operate also in DC and at low frequencies.
A program developed and upload inside the FPGA provides the comunication with all the devices of the generator; a wrire/read procedure permits to control the internal registers of the DAC as well as the internal register of both DDS devices implemeted at FPGA level.
Preliminary tests of the characteristics of the generator shows the possibility of operation for in the low frequency range and the a phase shift contained within 10 mrad up to 2 MHz.
Harmonic contribution of single tone ac synthesized signals by means of the DAC having an update rate of 1 Gsamples/second, from 50 kHz to 50 MHz, has a mean value of about 70 dB. The best performance are obtained at 500 kHz where the THD is about 0.02 %.
The rms output value of the DAC measured at various frequency shows a flat response up to 100 kHz. Beyond 100 kHz undesirable effects are due principally of the input structure of the measuring system and the connections plays an important role and in some case influence strongly the output of the DAC. Further

measurements will be undertaken in order to understand and solving some of the effects that influence directly the results.

V. Acknowledgment

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