

## Spectral Test of DAC Using Over Sampling and Low Resolution ADC

Domenico Luca Carnì, Domenico Grimaldi

*Department of Electronics, Computer and System Sciences,  
University of Calabria, 87036 Rende – CS, Italy  
Ph.: +39 0984 494712, Fax: +39 0984 494713, {dlcarni, grimaldi}@deis.unical.it*

**Abstract-** In the paper a new testing method for spectral analysis of DACs is presented. The method requires low resolution high speed ADC to acquire the resulting signal obtained by adding to the output voltage of the DAC under test the periodic voltage with sawtooth shape.

The zero crossing time sequence detected in the quantized signal is used to infer the value of the sawtooth voltage and, consequently, that of the output voltage of the DAC. Because the sampled signal is characterised by non-uniform sampling time, the spectral analysis is performed on the basis of a procedure pointed out to overcome the problem concerning the frequency ambiguities in the spectral analysis of non-uniformly sampled signal. This procedure permits the reconstruction of the uniformly sampled spectrum by starting from the non-uniformly sampled one.

The results of numerical test on 14-bit DAC by using 6 bit ADC were shown. Finally, the advantages of the method respect to another presented in literature, based on low resolution ADC and dithering, are discussed.

### 1. Introduction

Digital to Analog Converters (DACs) have growing use for applications such as wireless communications and interface between digital signal processing and analog signal. In spite of the efforts to develop methods for test the different types of DACs, testing remains an open problem for technicians and researchers [1]-[14]. Indeed, with the advancement in performance of the next generation DACs, there are new needs in testing. Both the static and the dynamic tests have become one of the most challenging problems [14].

On the basis of the demand arising from the manufacturers, a new test method is proposed in [14]. It is pointed out to address three goals: short test time, high test accuracy and low resolution measurement instruments. The test method is based on the use of low-resolution Analog to Digital Converter (ADC) and dithering to increase the resolution of the test. The result accuracy of the test is guaranteed by an effective data processing algorithm applied to the DAC output quantized voltage by the low resolution ADC.

The computational complexity of this algorithm increases as the resolution of the DAC under test increases respect to that of the ADC. In order to overcome this inconvenient, the research given in the paper is addressed to a different testing method based on a new approach. Fundamental aspect of this approach is that the problem of the signal acquisition with high resolution is shifted to the simpler problem of the high speed signal acquisition. A similar approach was presented in [15], [16] from the Authors for the static characterization of high resolution DAC. In the paper this approach is adapted and upgraded to point out the spectral analysis.

In particular, the method pointed out requires a low resolution high speed ADC to quantize the resulting signal obtained by adding to the output voltage of the DAC under test the periodic voltage with sawtooth shape. In the quantized signal the zero crossing time sequence is detected. This time sequence is used to infer the value of the sawtooth signal and, consequently, the corresponding value of the output voltage signal of the DAC.

This signal is characterised by the non-uniform sampling time. The spectral analysis by the Discrete Fourier Transform (DFT) of the non-uniform sampling time signal can be affected by ambiguities caused by the modulation effects described in [17]. In literature, the technique based on the reconstruction of the uniform sampled spectrum from that obtained by non-uniformly sampled signal is proposed in [18], [19]. This technique is based on the knowledge of the sampling time instants characterized by periodic non-uniformity into the sample period and it can be conveniently employed in the spectral analysis of the DAC.

The paper is organised as follows. The proposed method for the spectral test of DAC by using high speed low resolution ADC is presented. The procedure to reconstruct the uniform sampled spectrum from the non-uniformly sampled one is abstracted. Successively, the method validation is performed by means of numerical tests. Finally, the advantages respect to the method presented in [14] are discussed.

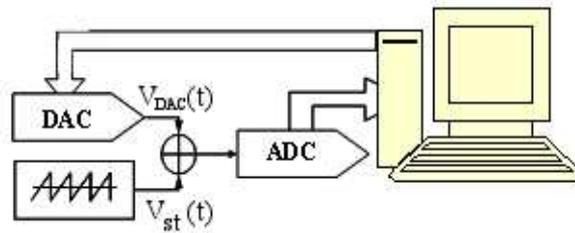


Figure 1. Equipment for the spectral test of DAC.

## II. The method for the spectral test of DAC

Fig. 1 shows the block scheme pointed out to execute the proposed test method. The PC feeds the DAC by means of the Digital Input Code (DIC), corresponding to the sinusoidal signal. The output voltage  $v_{DAC}(t)$  of the DAC under test is added to the sawtooth signal  $v_{st}(t)$  fed by high resolution generator. The resulting signal  $v_r(t) = v_{DAC}(t) + v_{st}(t)$  is over-sampled by the low resolution ADC and stored in the PC memory.

The ADC quantizes the amplitude of its input signal. This operation introduces at the output of the converter a quantization noise. In the frequency domain the quantization noise is characterized by a flat bandwidth and amplitude proportional to the resolution of the ADC. On the basis of this consideration is evident that the quantization noise introduced by the ADC to acquire the output signal must to be lower than the noise present at the output of the DAC. Usually, to obtain this condition the ADC has a resolution greater than that of the DAC. This condition is necessary to guaranty that the noise introduced by the acquisition system is lower than that characterising the DAC.

In the proposed test method the DAC output voltage is acquired not by codes of the ADC, but by using the zero crossing distribution in time of the resulting signal. Fig. 2 shows the resulting signal assuming:

$$v_{DAC}(t) = V_{DAC} \sin(\omega t + \varphi) \quad (1)$$

$$v_{st}(t) = 2V \left( f \cdot t - \text{floor} \left( f \cdot t + \frac{1}{2} \right) \right) \quad (2)$$

where  $f$  is the frequency and  $V$  is the amplitude of the sawtooth signal. The sawtooth voltage can be generated by another DAC with higher bit number than the DAC under test. Denoted by  $t_1, \dots, t_n$  the sequence of the  $n$  zero crossing time, the (2) permits to determine the value of the sawtooth voltage and, consequently, the corresponding value of  $V_{DAC}(t)$ .

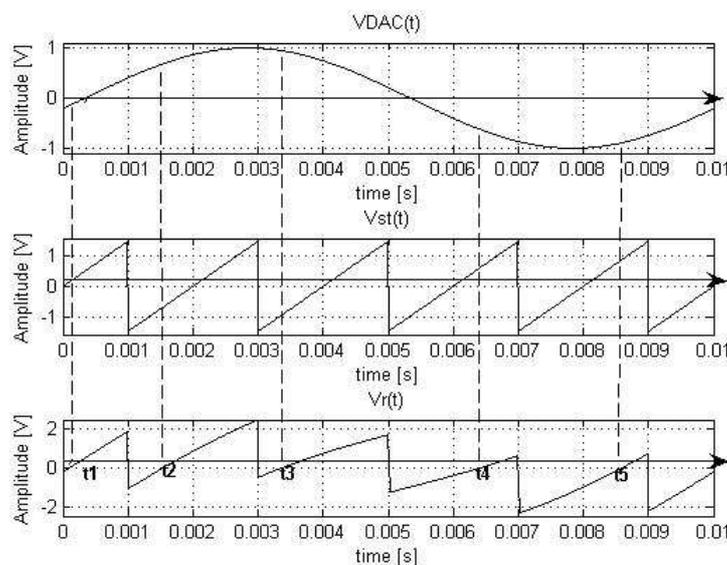


Figure 2. DAC output voltage (upper), sawtooth voltage (center), and resulting signal (down).  $t_1, \dots, t_n$  is the sequence of the  $n$  zero crossing time detected by the ADC.

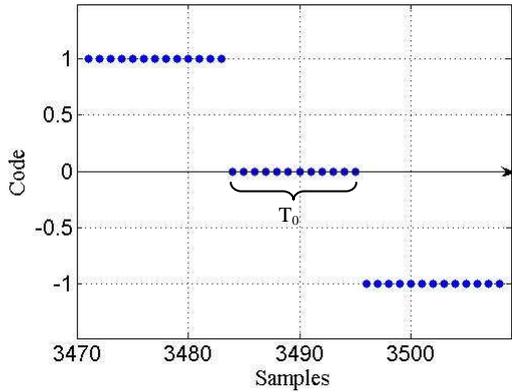


Figure 3. Samples with equal zero value into the time interval  $T_0$ .

### A. Zero crossing time detection

In general, none of  $n$  zero crossing time is coincident with the sampling time of the resulting signal  $v_r(t)$ . The position of each zero crossing time into the vector of the acquired samples can be estimated, only, by detecting the change of the sample sign.

When the acquired signal is over-sampled a group of samples with equal zero value can occurs as shown in Fig. 3. In this case, the estimation of the value of the zero crossing time is difficult because there are lack of information about the evolution of the signal in the time interval  $T_0$  defined by the samples with equal zero value. The non correct evaluation of the zero crossing time causes amplitude error for the evaluation of  $V_{DAC}(t)$ , and

reconstruction error of the uniform sampled spectrum from that obtained by non-uniformly sampled signal.

Many numerical techniques are available to estimate the zero crossing time. These are: (i) polynomial regression, (ii) spline interpolation, (iii) mean value of the time interval  $T_0$ , and (iv) first or last sample with zero value in the time interval  $T_0$ . In the following each of these techniques is taken into examination in order to highlight the vantage and the disadvantage in the framework of the proposed method.

The technique based on the polynomial regression or spline interpolation fail because there are lack of information about the evolution of the signal inside the time interval  $T_0$ . If samples before and after this interval are added in the numerical procedure, the error increases in the evaluation of the zero crossing time because they introduce information about the trend of the piecewise linear signal to be approximated, only, and non local information inside the time interval  $T_0$ .

The evaluation of the mean value of  $T_0$  can be accurate estimation of the zero crossing time only under the condition that the slope of the signal  $v_r(t)$  is constant in the time interval taken into account. This condition is not respected because the slope of  $v_r(t)$  is not constant in consequence of the fact that one of the summing signal is the sinusoidal signal  $v_{DAC}(t)$ .

The assumption of the zero crossing time in correspondence of the sampling time in which the first sample is equal to zero permits to overcome the difficulties of the previous numerical techniques. Indeed, at this sampling time the input signal crosses the ADC threshold equal to  $\pm Q/2$ , that represents the conventional value equal to zero for the ADC. Therefore, it is obviously to assume the zero crossing time corresponding to the first sampling time with zero value. In similar manner can be justified the choice of the last sample. The validation of the previous assumption is based on the fact that the best accurate results in the reconstruction of the spectrum are obtained. As a consequence of this zero crossing time evaluation, the amplitude offset corresponding to the value equal to  $Q/2$  into the reconstructed signal appears. This offset is not important into the spectral analysis of the ADC, because it increases only the spectral line amplitude to the zero frequency.

### III. Reconstruction of the uniformly sampled spectrum

In [19] is proposed a method for the reconstruction of the spectrum for a band-limited signal sampled with non-uniformly spaced time intervals. The situation considered is that the timing of each sampling instant of the acquired signal is known and has a periodic structure. Therefore, by considering  $n=kM+m$ , where  $k$  is in the range from  $-\infty$  to  $+\infty$  and  $m$  in the range from 0 to  $M-1$ , the sampling time sequence can be expressed as:

$$t_n = nT + \Delta_m = kMT + mT + r_m T \quad (3)$$

where  $T$  is the nominal sampling period,  $M$  is number of samples in a period of the non-uniform time sampling instant,  $\Delta_m$  the periodic sequence with period  $M$ . The parameter  $r_m$  is the normalization of  $\Delta_m$  to the nominal period:  $r_m = \Delta_m / T$ .

The computation of the spectrum from the signal  $x(t_n)$  gives as result the spectrum  $X_d(\omega)$  that is different from the spectrum of the same signal uniformly acquired  $X_c(\omega)$ . Considering that  $X_c(\omega)$  is band-limited in the range  $(-\pi/T, \pi/T)$ , it is possible to determine a relation between  $X_c(\omega)$  and  $X_d(\omega)$  into an arbitrary point

$\omega_0$ , with  $0 < \omega_0 < 2\pi/MT$ . This relation is the following:

$$TX_d(\omega_0 + 2\pi/MT) = \sum_{k=-M/2+1}^{M/2} A(k+1)X_c[\omega_0 - k(2\pi/MT)] \quad (4)$$

where:

$$A(k) = \frac{1}{M} \sum_{m=0}^{M-1} e^{-jkr_m(2\pi/M)} e^{-jkm(2\pi/M)} \quad (5)$$

The (4) can be expressed in a matrix form as:

$$TX_d(\omega_0) = A X_c(\omega_0) \quad (6)$$

The matrix A has dimension MxM and it can be quickly constructed thanks to the properties and repetition of its elements. From (6) it is possible to compute the M uniform bins of the uniformly sampled spectrum as:

$$X_c(\omega_0) = A^{-1} TX_d(\omega_0) \quad (7)$$

By using the (7) the reconstructed uniformly sampled spectrum of Fig 4b) is obtained from the non-uniformly sampled spectrum of Fig. 4a).

#### A Effect of the zero crossing time error on the reconstructed spectrum

In spite of the effort toward the accurate detection, the zero crossing time is affected by evaluation uncertainty that influences the spectrum reconstruction. In order to investigate about the effects on the reconstructed spectrum, the evaluation uncertainty has been taken into account as superimposed noise on the parameter  $r_m$  characterizing the non-uniform distribution of the sampling time respect to the uniform one. This noise is assumed random with mean value equal to zero and assigned peak value. Fig.5a) shows the reconstructed spectrum without superimposed noise to  $r_m$ , Fig.5b) and c) refer to superimposed noise with peak value equal to 1% and 10% of  $r_m$ , respectively. As expected, the noise floor in the reconstructed spectrum increases as increases the noise peak value. The effect of the increasing noise floor is the reduction of the bit number of the DAC that can be tested.

#### IV. Method validation

The method validation is performed in Matlab environmental by evaluating the Spurious-Free Dynamic Range (SFDR) of 14-bit DAC. The resulting signal  $v_r(t)$  is acquired by the ideal 6-bit ADC with sampling frequency  $f_s$  equal to 50MHz and full scale equal to 1,25V. The frequency of the DAC output signal  $V_{DAC}(t)$  is equal to 200Hz, and the amplitude is equal to 1V. For the sawtooth signal, the frequency is equal to 5kHz, and the amplitude is equal to 3.50V. Therefore, 400 samples are acquired and processed in the spectrum domain. Moreover, the Gaussian noise with standard deviation equal to 1 LSB, referred to 14-bit level, is added to the DAC output sine wave, and the SFDR is set equal to 80 dB.

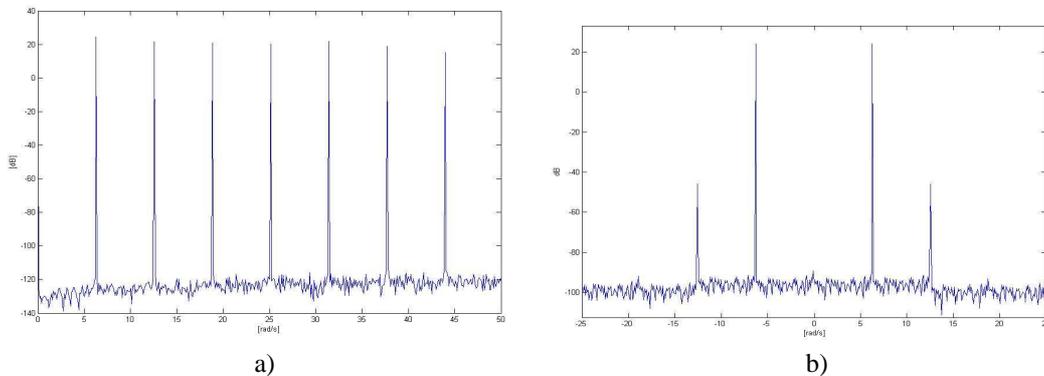


Figure 4. a) DAC non-uniformly sampled spectrum with  $r_m=80\%$ , and b) reconstructed uniformly sampled spectrum of signal sum of two sinusoidal signals at different frequency ( $f_1= 1\text{Hz}$ ,  $f_2= 2\text{Hz}$ ) and amplitude ( $V_1= 20\text{dB}$ ,  $V_2= -40\text{dB}$ ).

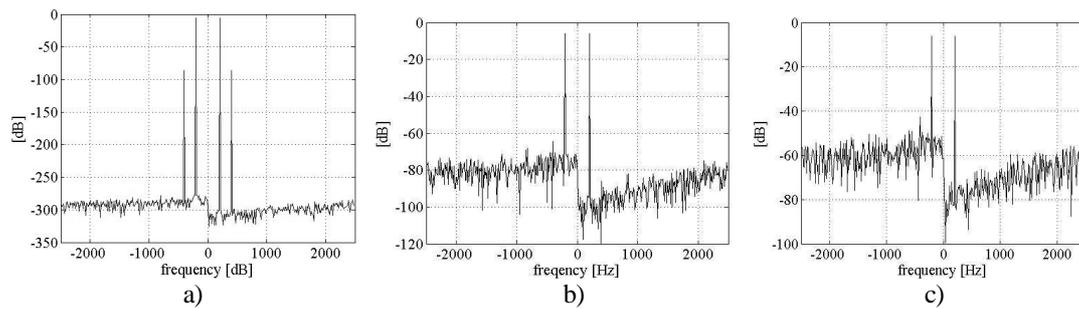


Figure 5. Reconstructed spectrum of signal sum of two sinusoidal signals at different frequency ( $f_1=200\text{Hz}$ ,  $f_2=400\text{Hz}$ ) and amplitude ( $V_1=0\text{dB}$ ,  $V_2=-80\text{dB}$ ), a) without superimposed noise to  $r_m$ , and with superimposed noise characterized by peak value equal to b) 1%, and c) 10% of  $r_m$ .

The spectrum estimated by the method is shown in Fig. 6. Fig.6a) shows the non-uniform sampled spectrum before the correction. Fig.6b) shows the reconstructed uniformly sampled spectrum. The SFDR estimated from Fig.6b) is equal to 79.89 dB. Therefore the evaluation error is equal to 0.11dB. This result shows that the proposed method is more accurate than that proposed in [14]. Indeed, the error shown in [14] is equal to 0.34dB in the same condition of the performed test.

Other tests are devoted to investigate about the trend of the error for the evaluation of increasing values of the SFDR. Therefore, the SFDR is estimated for different values of the spurious signal amplitude by considering (i) the uniformly sampled spectrum and (ii) the reconstructed uniformly sampled spectrum. The 14 bit DAC generating the sinusoidal signal with frequency equal to 200 Hz and amplitude equal to 1V is considered with superimposed spurious sinusoidal signal at different amplitude and random frequency in the range [300 Hz, 1kHz]. Always 400 samples are acquired by 6 bit ADC with sampling frequency equal to 200 MHz. The sawtooth signal is characterised by the frequency equal to 5 kHz and amplitude equal to 3.75 V. The error trend for the evaluation of the SFDR is shown in Fig.7. The results shown in this figure highlights that the proposed method guaranties the accuracy lower than 0.6 dB for the SFDR lower than 92 dB. For SFDR greater than 92 dB the amplitude of the spurious signal superimposed has the value near to the noise floor of the DAC, as a consequence the estimation error increases up to the value equal to 1.2 dB for SFDR equal to 95 dB.

Further comparison of these results with that shown in [14] highlights that the proposed method guaranties the accuracy lower than 0.55 dB for SFDR in the range [75 dB, 90 dB]. Differently, in the same range the error evaluated in [14] is lower than 1.5 dB.

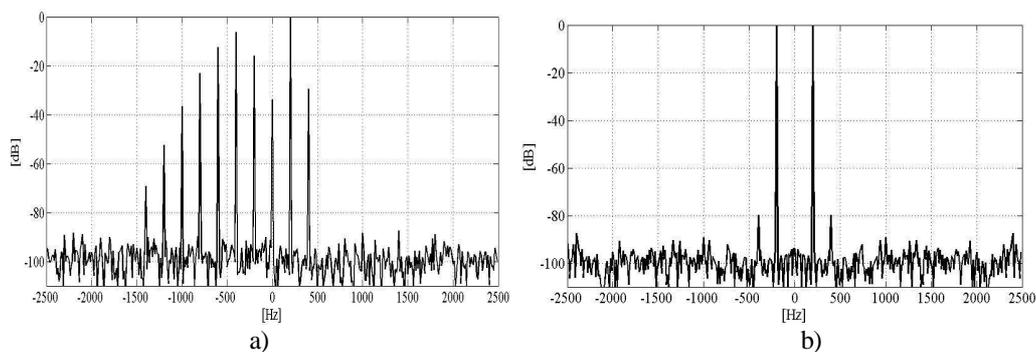


Figure 6. Spectrum with non-uniform sampling a) before the correction, and b) after the correction.

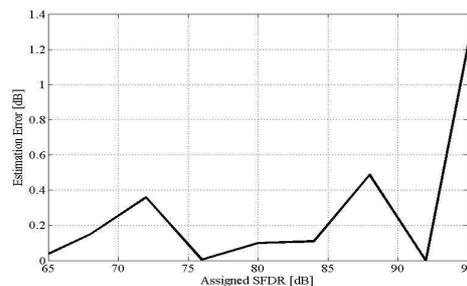


Figure 7. Error trend for the evaluation of the SFDR in the case of 14 bit DAC by using 6 bit ADC.

## V. Conclusions

A new testing method for spectral analysis of high resolution DACs is presented. The method requires low resolution high speed ADC to acquire the resulting signal obtained by adding to the output voltage of the DAC under test the periodic voltage with sawtooth shape.

The output of the DAC under test is evaluated by means of the zero crossing time detected in the quantized signal by the ADC. The particular technique to reduce the error in detecting the zero crossing time was experimented.

The signal obtained is characterised by the non-uniform sampling time. In order to overcome the problem concerning the frequency ambiguities, the spectrum domain analysis is performed on the basis of the technique that permits to reconstruct the uniform sampled spectrum from that obtained in the case of non-uniform sampling.

Moreover, the effect of the zero crossing time error is analysed on the reconstructed uniformly sampled spectrum of the signal.

On the basis of numerical tests the method validation is performed by considering the 14-bit DAC and the 6 bit ADC. Compared with another method presented in literature, based on low resolution ADC and dithering, the proposed method offer better accuracy. The analysis of the error trend has permitted to highlight the low level of accuracy that can be obtained in a wide amplitude range of the SFDR.

## References

- [1] J. Steensgaard, "High-resolution mismatch-shaping digital-to-analog converters", Proceeding of International Symposium on Circuits and Systems, ISCAS 2001, 6-9 May 2001, vol. 1, pp. 516–519.
- [2] International Technology Roadmap for Semiconductor, 2003 edition, available online at <http://public.itrs.net>.
- [3] B. Vargha, J. Schoukens, Y. Rolain, "Using reduced-order models in D/A converter testing", Proceeding of the 19th IEEE Instrum. and Measur. Technology Conference, Anchorage (USA), 21-23 May 2002, vol.1, pp. 701-706.
- [4] M. Burns, G. W. Roberts, "An introduction to mixed-signal IC test and measurement", Oxford series in Electrical and Computer Engineering. Oxford University Press, New York, 1<sup>st</sup> edition, 2001.
- [5] I.H.S. Hassan, K. Arabi, B. Kaminska, "Testing digital to analog converters based on oscillation-test strategy using sigma-delta modulation", Proceedings of International Conference on Computer Design: VLSI in Computers and Processors ICCD '98, 5-7 Oct. 1998, pp. 40-46.
- [6] X. Hanqing, C. Degang, R. Geiger, "Linearity test for high resolution DACs using low-accuracy DDEM flash ADCs", Proceedings of IEEE Intern. Symp. on Circuits and Systems ISCAS 2006, 21-24 May 2006.
- [7] S. Max, "Optimum DAC and ADC Testing", Proceedings of Instrumentation and Measurement Technology Conference IMTC 2008, 12-15 May 2008, pp. 573-578.
- [8] E. Balestrieri, "DAC Time-Domain specifications toward standardization" ", IEEE Transactions on Instrumentation and Measurement, vol.57, No.7, July 2008, pp. 1290-1297.
- [9] B. Jasper, "Practical telecom DAC testing", Available on line at: <http://www.testedgeinc.com>.
- [10] J. Savoj, Ali-Azam Abbasfar, A. Amirkhany, B.W. Garlepp, M.A. Horowitz, "A new technique for characterization of Digital-to-Analog Converters in high-speed systems" Design, Automation & Test in Europe Conference & Exhibition, DATE '07, 16-20 April 2007, pp. 1-6.
- [11] P.P. Fasang, "Optimal selection of test vectors for DA converter testing," Measur., vol.31,2002, pp.165–174.
- [12] L. Angrisani, M. Dapuzzo, M. D'Arco, "A new approach to linearity and intermodulation errors estimation in digital-to-analogue converters," Proceeding of 9th Workshop on ADC Modelling and Testing, Athens, Greece, Sep./Oct. 2004, vol. 2, pp. 859–864.
- [13] K. Arabi, B. Kamiska, M. Sawan, "On chip testing data converters using static parameters," IEEE Trans. Very Large Scale Integration (VLSI) System, vol. 6, no. 3, pp. 409–419, Sep. 1998.
- [14] J. Le, H. Hosam, R. Geiger, C. Degang, "Testing of precision DACs using low-resolution ADCs with dithering", Proceeding of IEEE International Test Conference, Oct. 2006, pp.1-10.
- [15] D.L. Carnì, D. Grimaldi, "Static characterization of high resolution DAC based on over sampling and low resolution ADC", Proc. of IEEE Instrum. and Measur. Techn. Conf., IMTC 2007, Warsaw, Poland, May 1-3, 2007.
- [16] D.L. Carnì, D. Grimaldi, "Over sampling method for the static characterization of high resolution DAC: a proposal for the IEEE Standard P1658", Proc. of IMEKO 12<sup>th</sup> Workshop on ADC Model and Testing, Iași – Romania, Sept.19-21, 2007.
- [17] M. Bellanger, "Digital processing of signals", Wiley, 2000.
- [18] Y.C. Jenq, "Perfect reconstruction of digital spectrum from non-uniformly sampled signals", IEEE Transactions on Instrumentation and Measurement, vol.46, No.3, June 1997, pp. 649-652.
- [19] Y.C. Jenq, L. Cheng, "Digital spectrum of a non-uniformly sampled two-dimensional signal and its reconstruction", IEEE Transactions on Instrum. and Measur., vol.54, No.3, June 2005, pp. 1180-1187.