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A Maximum Likelihood Estimator for ADC and DAC Linearity Testing

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***Abstract*-**The paper illustrates a method for simultaneous ADC and DAC linearity testing in a loop-back scheme. The main features of the method are: (i) it is statistically nearly optimal, being based on a maximum likelihood estimator; (ii) it does not require prior knowledge neither of the ADC nonlinearity, nor of the DAC nonlinearity – both are simultaneously measured relying only on a constant-variance noise. The performances of the method are studied both mathematically and via computer simulations. The method, because of its optimality and universality, appears to be also a good candidate for inclusion in technical standards relevant to ADC and DAC testing.

I. Introduction

As performances of analog-to-digital and digital-to-analog converters (ADCs, DACs) increase, testing becomes a more and more demanding task. ADC and DAC testing is of course necessary for verifying the fulfillment of specifications, either in the production line or in the laboratory of a final user. But testing is nowadays also necessary in order to obtain, and maintain, a certain level of performance in the conversion, due to the widespread use of digital linearization algorithm (a practical example in commercial devices is the NI-MCal calibration algorithm [1]). In general, it makes sense to manufacture an ADC with very high nominal resolution but large linearity errors, and increase the final performances by means of self-calibration and correction techniques. For example, the commercial ADC ADS1281 [2], which has a typical INL of 0.6ppm of FSR (for a data rate of 1000 samples per second), can output 32-bit as well as 24-bit readings. On the nominal 32-bit quantization scale, that INL corresponds to about 2600 LSB, whereas on the 24-bit quantization scale, it corresponds to about 10 LSB: the potentialities of digital error correction are apparent.

When the testing hardware is embedded in the device, we are in presence of BIST strategies, and among BIST schemes, those based on loop-back (where an ADC is stimulated by the dithered outputs of a DAC [3, 4]) are particularly promising. This scheme has a minimal hardware overhead in systems which already contains both kinds of converters. Test data consist in a table of code occurrences, which counts how many time a given code converted by the DAC results in a given output code from the ADC. This is a static test, because each DAC output code is maintained during repeated measurements with the ADC. In comparison with other ADC tests, where ramp [5] or sinusoidal [6, 7] or large Gaussian signals [8] are used, this test is immune from dynamical effects due to large signal variations and/or sampling time errors.

Of course the nonlinearity of the test signal generator is an issue when testing high resolution ADCs. In the context of loop-back test methods, this issue has been faced in several ways. As concerns ADC tests, a first set of methods relies on the knowledge of the DAC nonlinearity [3, 9, 10, 11]. The teaching is that an ADC can be tested using a DAC which hasn't higher resolution nor better accuracy, provided that the DAC has been externally characterized someway. In a second approach, instead, the nonlinearities of both the ADC and the DAC are measured at the same time [4]. This demonstrates that, as regards linearity testing, there is no need for any external reference instrument at all. This concept is put in practice, for example, in the instrument described in [1], which allows two kinds of calibrations to be performed: the external one is made, as usual, against a voltage standard, while the internal self-calibration relies only on the on-board hardware, and allows the correction of nonlinearities. The self-calibration in [1], however, accounts only for large scale nonlinearities (a third-order polynomial is used to approximate the nonlinearity), whereas the method presented in [4], which works at the LSB level (all the ADC thresholds and DAC output levels are estimated), is not theoretically optimal (the same accuracy could be reached with fewer measurements).

The aim of this paper is to demonstrate a new and efficient method for the simultaneous

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measurement of ADC and DAC nonlinearities in a loop-back test set-up. The method is near to the optimum, from the statistical point of view, because is based on the maximum likelihood (ML) estimation of ADC thresholds and DAC outputs. The illustrated technique is a generalization of the method presented in [10, 11] by the same authors.

The paper is structured as follows. In Section II the ML estimation algorithm is illustrated. In Section III simulation results obtained with the illustrated method are reported. In Section IV the statistical properties of the ML estimator are derived, by computing the Cramer-Rao lower bound (CRLB) for the estimation problem. In Section V are the conclusions and a summary of future work.

II. Derivation of the ML estimator

The first step toward the derivation of the ML estimator is to find the statistical model behind the test data. Let $\mathbf{x}=\left[x_1,x_2,...,x_M\right]^{\mathrm{T}}$ be a vector describing the M possible mean outputs of the DAC. It is assumed $x_1<x_2<...<x_M$. The ADC, in turn, is described by K code transition levels $\mathbf{t}=\left[t_1,t_2,...,t_K\right]^{\mathrm{T}}$, with $t_1<t_2<...<t_K$. Each DAC output is measured for N times by the ADC. At the nth conversion of the ith signal, the ADC input is modeled as a random variable X_i^n, which is assumed to be normally distributed as $N\left(x_i,\sigma^2\right)$. It is useful, at this point, to define the random variables $B_{i,k}^n$, which indicate if the kth ADC code is hit or not in the nth conversion of the ith signal. It is $B_{i,k}^n=1$ iff $t_{k-1}<X_i^n\le t_k$, with $k=1,...,K+1$, and $B_{i,k}^n=0$ otherwise. For consistency, we pose conventionally $t_0=-\infty$ and $t_{K+1}=+\infty$. It is assumed that $B_{i,k}^n$ are independent in the indexes i and n. What we are interested in is the table of code occurrences, which can be defined as an $M\times K+1$ random matrix $\mathbf{F}$ whose elements are $F_{i,k}=\frac{1}{N}\sum_{n=1}^{N}B_{i,k}^n$. The test data consist in the matrix $\mathbf{f}=\left[f_{i,k}\right]$ of observed relative frequencies, realization of $\mathbf{F}$. $\mathbf{f}$ satisfies the following conditions, which we will assume valid everywhere: $f_{i,k}\in\{0,1/N,2/N,...,1\}$; $\sum_{k=1}^{K+1}f_{i,k}=1$. The estimation problem is stated as follows: obtain the values of $\mathbf{x}$ and $\mathbf{t}$ starting from $\mathbf{f}$. It is preferable to collect $\mathbf{x}$ and $\mathbf{t}$ into a single column vector $\boldsymbol{\theta}_{\mathrm{FULL}}=[\mathbf{t};\mathbf{x}]$.

The probability of observing $\mathbf{f}$ given $\boldsymbol{\theta}_{\mathrm{FULL}}$ is the product of M multinomial distributions,

$$\mathrm{P}\left(\mathbf{F}=\mathbf{f};\boldsymbol{\theta}_{\mathrm{FULL}}\right)=\prod_{i=1}^{M}N!\prod_{k=1}^{K+1}\frac{1}{(Nf_{i,k})!}p_{i,k}^{Nf_{i,k}}(\boldsymbol{\theta}_{\mathrm{FULL}}), \tag{1}$$

where

$$\mathrm{p}_{i,k}([\mathbf{t};\mathbf{x}])=\Phi_{i,k}([\mathbf{t};\mathbf{x}])-\Phi_{i,k-1}([\mathbf{t};\mathbf{x}]) \text{ and } \Phi_{i,k}([\mathbf{t};\mathbf{x}])=\Phi\left(\frac{t_k-x_i}{\sigma}\right). \tag{2}$$

For consistency, we pose explicitly $\mathrm{p}_{i,1}=\Phi_{i,1}$ and $\mathrm{p}_{i,K+1}=1-\Phi_{i,K}$. We define also $\varphi_{i,k}([\mathbf{t};\mathbf{x}])=\varphi\left(\frac{t_k-x_i}{\sigma}\right)$.

In order to proceed to the estimation, we must note that the code occurrence data $\mathbf{f}$ allows the determination of $\mathbf{x}$ and $\mathbf{t}$ less than an offset and a scale factor. This is due to the structure of (2). For this reason we put, without loss of generality, $\sigma=1$, and we assume that the αth element in $\boldsymbol{\theta}_{\mathrm{FULL}}$ is known. Let $\boldsymbol{\theta}$ be $\boldsymbol{\theta}_{\mathrm{FULL}}$ without the αth element, that is $\boldsymbol{\theta}=\boldsymbol{\theta}_{\mathrm{FULL}}[1:\alpha-1,\alpha+1:K+M]$. At this point we can calculate the ML estimator of $\boldsymbol{\theta}$, $\hat{\boldsymbol{\Theta}}$, and the estimate $\hat{\boldsymbol{\theta}}$. They can be expressed formally as

$$\hat{\boldsymbol{\Theta}}=\mathbf{g}\left(\mathbf{F}\right),\ \hat{\boldsymbol{\theta}}=\mathbf{g}\left(\mathbf{f}\right) \tag{3}$$

where, by definition of ML estimation, it is $\mathbf{g}\left(\mathbf{f}\right)=\arg\max_{\boldsymbol{\theta}'}\mathrm{P}\left(\mathbf{f};[\theta'_1;...;\theta'_{\alpha-1};\theta_{\mathrm{FULL}\alpha};\theta'_{\alpha+1};...;\theta'_{K+M}]\right)$. By calculating the logarithm of (1), the following equivalent equation is obtained:

$$\mathbf{g}(\mathbf{f}) = \arg\max_{\boldsymbol{\theta}'} p'(\mathbf{f};[\theta'_1;...;\theta'_{\alpha-1};\theta_{\mathrm{FULL}\alpha};\theta'_{\alpha+1};...;\theta'_{K+M}]) , \quad (4)$$

where

$$\mathrm{p}'(\mathbf{f};[\mathbf{t}';\mathbf{x}']) = \sum_{\substack{i=1,...,M \\ k=1,...,K+1}} f_{i,k} \log p_{i,k}([\mathbf{t}',\mathbf{x}']) . \quad (5)$$

It is clear that the theoretical framework illustrated here can be applied to a larger set of problems. As an example, we can consider the case in which a DAC is tested by using a reference ADC. In this case Eq. (4) must be solved only for the DAC output levels, being the ADC thresholds known. Eq. (4) can also be generalized further, allowing that each DAC level was dithered by a different amount of noise, σ_i. This approach is currently under development and will not be reported in this paper. Finally, we argue that the ML estimation of ADC thresholds and of dithered and quantized signals is a technique useful far beyond the particular method illustrated here. For example in [12] it has been used to improve the ADC linearity test based on the three-parameters sine wave fitting. In [12] the model beyond the test data is that of a dithered sinusoid, and the ML estimation is used for the determination of the ADC thresholds as well as sinusoid parameters.

III. Simulation results

The method has been verified by means of simulations and hypothesizing several test conditions. For the sake of conciseness we report only a few of them, differing for the number of ADC samples per DAC code, $N = 2000$ or $N = 10000$, and for the amount of additive Gaussian noise that dithers the DAC output, $\sigma = 1$ LSB or $\sigma = 8$ LSB. In all the reported virtual experiments, an 8-bit ADC and an 8-bit-DAC with the same nominal quantization step have been used.

The ADC code transition levels and the DAC output levels have been estimated as described by Eqs. (3) and (4), assuming that the know parameter is $t_1 = 0$. In this first implementation of the method the numerical maximization has been performed by using the simplex method in the MATLAB programming environment.

The results are shown in Fig. 1, 2,3 and 4 for the case $N = 10000$ and $\sigma = 1$ LSB, in Fig. 5 and 6 for the case $N = 2000$ and $\sigma = 1$ LSB, and in Fig. 7 and 8 for the case $N = 10000$ and $\sigma = 8$ LSB. The estimation error is evaluated as the difference between the estimated and the true integral nonlinearity (INL). The performances of the method depend on several parameters, K, M, N, σ, and on the ADC and DAC quantization step. Preliminary results have shown that the estimation error has a dependence on N of the kind $1/\sqrt{N}$. Moreover, the error in the estimation of the ADC INL exhibits little dependence on σ for values of σ above 1 LSB.

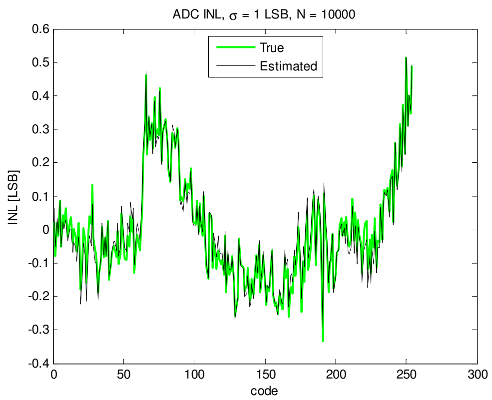

Figure 1. Comparison between the estimated and true ADC INL.

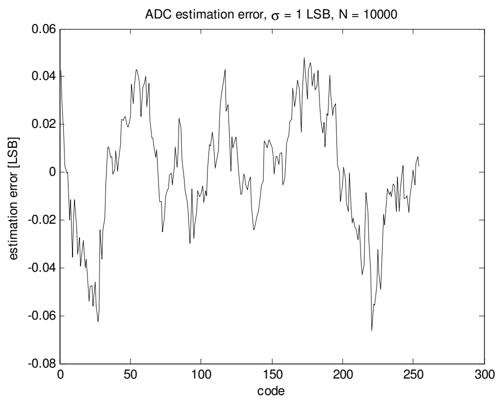

Figure 2. Error in the estimation of the ADC INL.

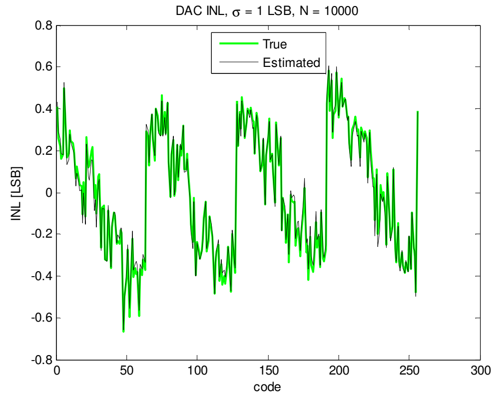

Figure 3. Comparison between the estimated and true DAC INL.

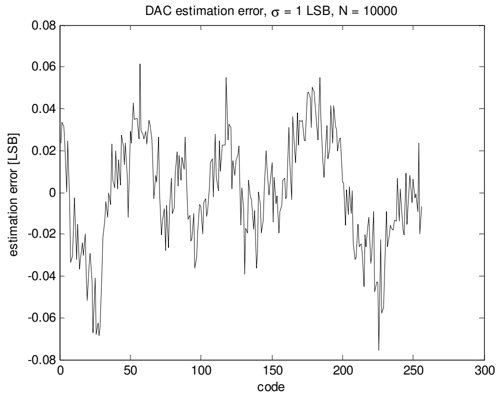

Figure 4. Error in the estimation of the DAC INL.

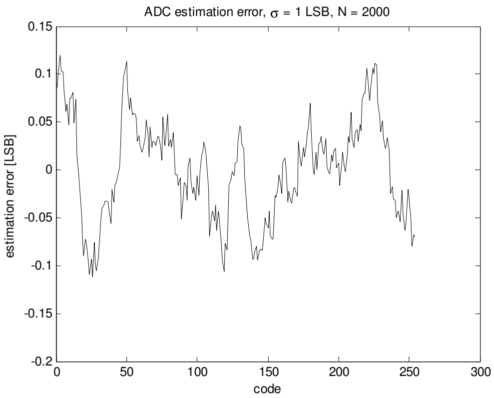

Figure 5. Error in the estimation of the ADC INL.

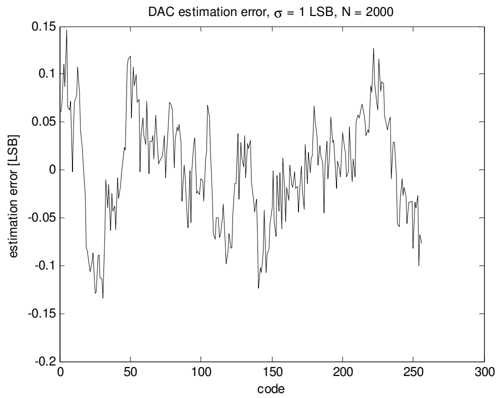

Figure 6. Error in the estimation of the DAC INL.

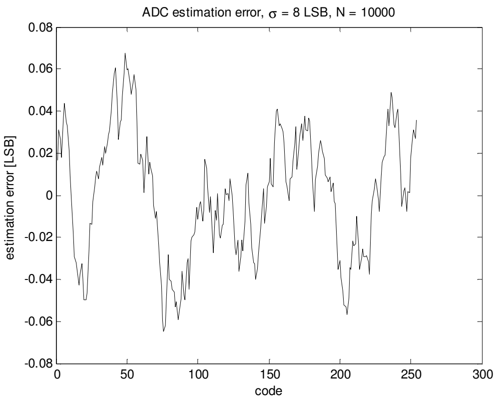

Figure 7. Error in the estimation of the ADC INL.

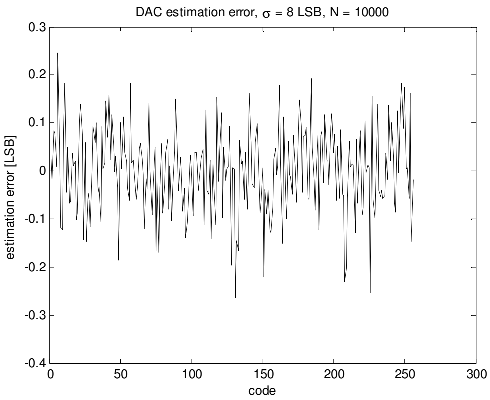

Figure 8. Error in the estimation of the DAC INL.

IV. Statistical properties

The bias and the covariance of $\hat{\mathbf{\Theta}}$ can be calculated on the basis of Eq. (3). However, as a general property, ML estimators are asymptotically unbiased and efficient. For this reason, we have calculated the CRLB, $\mathbf{I}^{-1}(\boldsymbol{\theta}_{\text{FULL}},\sigma)$. The diagonal of $\mathbf{I}^{-1}(\boldsymbol{\theta}_{\text{FULL}},\sigma)$ is an useful approximation of the estimator variance. The DAC and ADC transfer functions are often expressed in terms of INL. Being the DAC and ADC INLs a transformation of the parameters $\boldsymbol{\theta}_{\text{FULL}}$, the statistical properties of the ML estimators of both INLs are functions of the statistical properties of the ML estimator $\hat{\mathbf{\Theta}}$.

In calculating the Fisher information matrix $\mathbf{I}(\boldsymbol{\theta}_{\text{FULL}},\sigma)$, we consider that one of the parameters, $\boldsymbol{\theta}_{\text{FULL}}[\alpha]$, is known and has not been included among the parameters to be estimated. It is useful to consider $\mathbf{I}(\boldsymbol{\theta}_{\text{FULL}},\sigma)$ as extracted from a larger matrix, where in the extraction all columns and rows are selected except for the αth. We denote this extraction operation by using the subscripted reference $[:-\{\alpha\},:-\{\alpha\}]$. It has been obtained that $\mathbf{I}(\boldsymbol{\theta}_{\text{FULL}},\sigma)$ has the following structure:

$$\mathbf{I}(\boldsymbol{\theta}_{\text{FULL}},\sigma)=\frac{N}{\sigma^2}\begin{bmatrix}\mathbf{A} & \mathbf{B}^{\text{T}}\\ \mathbf{B} & \mathbf{C}\end{bmatrix}_{[:-\{\alpha\},:-\{\alpha\}]}, \tag{6}$$

where $\underset{K\times K}{\mathbf{A}}$ is a symmetric tridiagonal matrix, $\underset{M\times K}{\mathbf{B}}$ a full matrix and $\underset{M\times M}{\mathbf{C}}$ a diagonal one, with $\mathbf{A}_{k,k}=\sum_{i=1}^{M}\varphi_{i,k}^2\left(\frac{1}{p_{i,k}}+\frac{1}{p_{i,k+1}}\right)$, $\mathbf{A}_{k,k+1}=-\sum_{i=1}^{M}\frac{\varphi_{i,k}\varphi_{i,k+1}}{p_{i,k+1}}$, $\mathbf{B}_{i,k}=\varphi_{i,k}\left(\frac{\varphi_{i,k+1}-\varphi_{i,k}}{p_{i,k+1}}-\frac{\varphi_{i,k}-\varphi_{i,k-1}}{p_{i,k}}\right)$, $\mathbf{C}_{i,i}=\sum_{k=1}^{K+1}\frac{\left(\varphi_{i,k}-\varphi_{i,k-1}\right)^2}{p_{i,k}}$. It is implicitly assumed that all the functions φ and p are calculated in $\boldsymbol{\theta}_{\text{FULL}}$.

The CRLB for the estimation of the DAC and ADC INLs can be derived from the CRLB for the estimation of the parameters $\mathbf{t}$ and $\mathbf{x}$. The INLs have been defined as

$$\mathbf{INL}_{\text{ADC}}=\frac{\mathbf{t}-G_{\text{ADC}}\tilde{\mathbf{t}}-O_{\text{ADC}}}{G_{\text{ADC}}},\ \mathbf{INL}_{\text{DAC}}=\frac{\mathbf{x}-G_{\text{DAC}}\tilde{\mathbf{x}}-O_{\text{DAC}}}{G_{\text{DAC}}}, \tag{7}$$

where $\tilde{\mathbf{t}}=[0,...,K-1]-(K-1)/2$ and $\tilde{\mathbf{x}}=[0,...,M-1]-(M-1)/2$. The coefficients G and O are obtained by minimizing $\left\|\mathbf{t}-G_{\text{ADC}}\tilde{\mathbf{t}}-O_{\text{ADC}}\right\|$ and $\left\|\mathbf{x}-G_{\text{DAC}}\tilde{\mathbf{x}}-O_{\text{DAC}}\right\|$. For the sake of conciseness, we define $\mathbf{INL}=[\mathbf{INL}_{\text{ADC}};\mathbf{INL}_{\text{DAC}}]$. The CRLB of the INL, $\mathbf{I}_{\text{INL}}^{-1}(\mathbf{INL},\sigma)$, is given by

$$\mathbf{I}_{\text{INL}}^{-1}(\mathbf{INL},\sigma)=\left(\frac{\partial\mathbf{INL}}{\partial\boldsymbol{\theta}_{\text{FULL}}}\right)_{[:,:-\{\alpha\}]}\mathbf{I}^{-1}(\boldsymbol{\theta}_{\text{FULL}},\sigma)\left(\frac{\partial\mathbf{INL}}{\partial\boldsymbol{\theta}_{\text{FULL}}}^{\text{T}}\right)_{[:-\{\alpha\},:]}, \tag{8}$$

where the subscripted references $[:,:-\{\alpha\}]$ and $[:-\{\alpha\},:]$ indicate the deletion of the αth column and row, respectively.

Equation (8) can be used to design the test after the choose of a desired uncertainty, in the assumption that the ML estimator is near to being efficient. The variance in the ML estimation of all the elements of the INL, in a given test condition specified by the parameters $\mathbf{t}$, $\mathbf{x}$, σ and N, can be found on the diagonal of $\mathbf{I}_{\text{INL}}^{-1}(\mathbf{INL},\sigma)$. In practical calculations, $\mathbf{t}$ and $\mathbf{x}$ can be substituted by their nominal values.

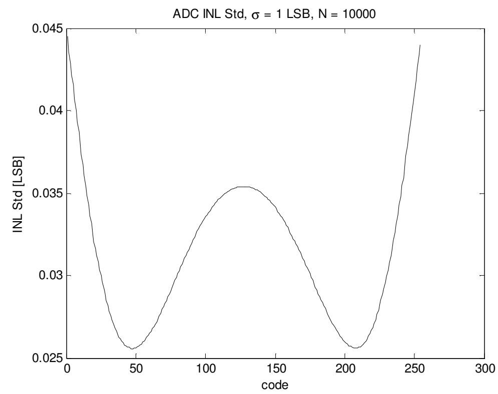

Figure 9. Estimator standard deviation for the ADC INL

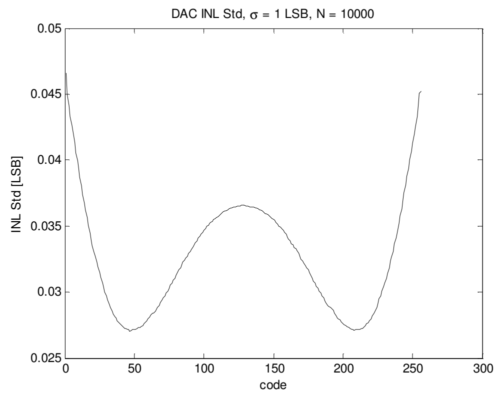

Figure 10. Estimator standard deviation for the DAC INL.

Figures 9 and 10 report the standard deviation of the INL estimators, derived from the CRLB calculated in the same test conditions as of Figures 2 and 4. These results of the CRLB computations are compatible with the errors reported in Figures 2 and 4.

V. Conclusions

A method has been presented for testing ADCs and DACs in a loop-back scheme. It is based on an ML estimator, and it relies only on a small Gaussian noise acting as a dither signal. If the dither signal is actually Gaussian, zero-mean and with constant (even if unknown) variance, the nonlinearity of both the ADC and the DAC are estimated in a nearly optimal way.

The method is particularly suitable for effective implementing of a BIST strategy. It is clear, besides, that several problems can be addressed within the same theoretical framework illustrated in the paper: ADC linearity testing using a reference DAC; DAC linearity testing using a reference ADC; contemporaneous ADC and DAC testing [this paper]; and, finally, transfer of accuracy between ADCs and/or DACs.

The method can be seen as an improvement and a generalization of the loop-back ADC testing scheme described in the IEEE Standard for ADCs [7]. It can be easily implemented also for testing stand-alone waveform recorders like digital oscilloscopes, addressed in the IEEE Standard [6]. And of course it is applicable to DAC testing, addressed in the draft Standard [13]. Therefore, it seems reasonable to consider it for a future inclusion in one or more of such Standards.

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