13th Workshop on ADC Modelling and Testing
Sep. 22-24, 2008, Florence, Italy

Optimized Decimation Structure for Complex Bandpass ΣΔ Modulator in Wideband Receiver

Haïfa FARES [1], Chiheb REBAI [1], Bertrand LE GAL [2], Dominique DALLET [2]

[1] *CIRTA'COM research unit High school of Communications SUP'COM, Tunisia*
chiheb.rebai@supcom.rnu.tn

[2] *IMS Laboratory – ENSEIRB Université de Bordeaux I, France*
dominique.dallet@ims-bordeaux.fr

Abstract- This paper presents an efficient design of a decimation filter for a continuous-time (CT) complex bandpass ΔΣ modulator in wideband-standards receiver. The RF front-end has been based on a modified low-IF architecture and the full receiver dynamic range is converted into the digital domain. The approach proposed investigates a new decimation process and realizes new functionalities such as image rejection and frequency down conversion IF/DC by a complex mixing on ΔΣ modulator bit stream. Two wide standards (IEEE 802.11a and 802.16) were chosen for design procedure illustration. The decimation structure was implemented on FPGA component using optimization techniques. Experimental results show the high-speed data rate and low-power consumption features of the proposed design.

I. Introduction

The development of a Software radio system implies the achievement of two main goals. The first is to implement a small, low-cost and low power transceiver. The second is to handle multiple digital communication standards in a single chip solution. Many research work results let possible the design of analog RF/IF components that process such signals [1]. However, the analog to digital converter (ADC) stills a critical component in software radio terminal in terms of dynamic range and sampling frequency regarding multi-standard requirements. Under this situation, ΔΣ ADC becomes one of the most suitable architecture. Furthermore, CT ΔΣ modulators are suited for a low-cost integration because they provide anti-aliasing filtering without silicon-area penalty and can potentially operate with less power consumption than discrete-time implementation [2] [3]. In addition, using a bandpass instead of lowpass ΔΣ modulator aims at a high degree of digitization by placing mixing operations in digital domain. There are some tradeoffs in the whole receiver system design between the decimation filter and other processing stage like for instance the image rejection block. This work will give an overview on the considerations of the decimation filter design based on two popular standards, including 802.11a and WiMAX. In section II, the proposed receiver architecture is described showing modification introduced over Low - IF structure in order to increase its reconfiguration flexibility. Section III provides receiver specifications for the two considered standards. Next, the crucial functionalities in the decimation filter design are analyzed in order to draw the desired decimation structure. Implementation and circuit level optimizations are discussed in section V. Then experimental results are presented before drawing conclusions in Section VI.

II. Proposed receiver architecture

The Low-IF receiver architecture, with modern quadrature mixers and strategic IF placement, offers a viable solution for realizing digital, monolotic receiver. Indeed, Low-IF receiver combines the advantages of both the heterodyne and homodyne receivers [4]. The RF signal is not down converted to DC but to a frequency band close to DC, called Low-IF band. The problem of DC offset and flicker noise of homodyne receiver does not arise. This receiver, for specific modulation schemes, is preferred for high integration and easy-made. However, since the image signal comes again from another channel with a possible high power level, this work has explored the possibility of introducing image rejection block in digital domain within decimation process after digitizing the IF signal with an oversampled bandpass $\Delta\Sigma$ modulator. The use of bandpass ΔΣ modulator permits the direct conversion of an analog signal to digital format at IF frequencies and allows the digital in phase-quadrature (I/Q) mix which reduces the problem of gain/phase mismatches [5]. Therefore, CT ΔΣ modulators have the advantage over their counterpart discrete-time (DT) ΔΣ modulator that there is no need for additional analog Anti - Aliasing Filter (AAF). Furthermore, a CT ΔΣ modulator achieving a large dynamic

range, excellent linearity and built-in filtering for out of band channel interferes is proposed in [6]. Moreover, with this architecture it has been shown that no Automatic Gain Control (AGC) blocks are required to reduce the receiver dynamic range.

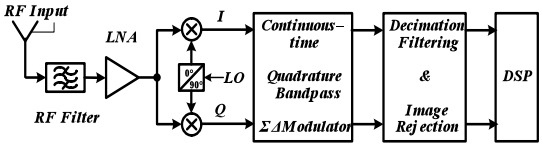

Figure 1. Highly digitized Low-IF receiver

The decimation filtering is done in IF and a down conversion to baseband should be performed on the decimated signal. The complex bandpass filters perform decimation, image rejection and transforms the complex signal to a real signal. The final scheme of the proposed receiver architecture is shown in Figure 1. To illustrate the multi-standard flair, two standards, IEEE 802.11a and IEEE 802.16, are specified in the next section for the proposed receiver.

III. RF Front End Design

The RF specifications used in this work are a combination of the specifications extracted from Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications of both IEEE 802.11a - 1999 [7] and IEEE 802.16 - 2000[8]. The objective of this section is to compute receiver design parameters by considering Wi-Max and Wi-Fi standards specifications in order to have baseband decimation filter specifications. Standards parameters are summarized in table 1.

Parameters	Wi-Max	Wi-Fi
Transmission bands	2 - 11 GHz 5.15 - 5.35 GHz	5.15 - 5.35 GHz 5.725 - 5.825 GHz
Channel Width (BW)	19.25 MHz	16.6 MHz
Channel Spacing	20 MHz	
Reference Sensitivity (S_{Ref})	-65 dBm for 54 Mbps	-65 dBm
Maximum Received Power (S_{max})	-30 dBm	-30 dBm
Received Signal to Noise Ratio at Antenna (SNR_{in})	37 dB	36.8 dB
Signal to Noise Ratio after receiver processing (SNR_{out})	30 dB	26.8 dB
Maximum Blocker Level (Nbl_{max})	-39 dBm	-47 dBm

Table 1. IEEE 802.16 and IEEE 802.11a Receiver Specifications

The sampling frequency was set to 160 MHz in order to obtain a reasonable OSR for the 20 MHz bandwidth. A design methodology for Low-IF Front – End was detailed in [9] and used in this work. Receiver specifications in terms of dynamic range, noise and linearity are given in Table 2 for the both standards. The multi-standard receiver parameters are chosen to meet severe parameters for both standards.

Standards	WLANa	WiMax
Noise Figure NF (dB)	16.67	11.58
Analog Gain (dB)	43	43
IIP3 (dBm)	-4.34	-1.8
ADC Dynamic Range (dB)	54.31	59.4

Table 2. Design Specifications

IV. Proposed Decimation Scheme

In this section, we detail the proposed approach for digital filtering strategy in baseband.

A. Decimation structure

In this new decimation structure, for saving power advantage, we conserve multistage design replacing single decimation filter by cascaded filters. The bandpass NTF stopband is not centered on DC but on a

non-zero frequency f_0 that is well removed from DC, such as $f_0 = F_s/4$. Many modifications are introduced over classical decimation filters to overlap restrictions on the design of receiver system. First is the use of bandpass ΔΣ modulator instead of lowpass one. Both convert an analog signal between the two is in the shape of the Noise transfer Functions (NTF).
Secondly, in order to be compatible with other narrow-band radio receiver system, the decimation digital filtering section was required to be placed before the baseband down conversion stage in the signal chain. The need, therefore, was for architecture to perform narrowband complex filtering at IF.
Thirdly, as the hardware is tied to the choice of ω_0, a constant value of $\omega_0 = \pi/2, \pi/4$ at the down conversion mixer can be ensured, so that the design complexity can be shifted from the complexity of the PLL design to the good choice of high order ΔΣ modulator.
Figure 3 shows the block diagram of decimation structure using complex CT ΔΣ bandapss modulator. This decimation structure performs:

- Anti-alias filtering and reduction of the data rate
- Attenuation of remaining out of band spurious
- Image rejection and generation of a real two sided signal centered around $\pm F_{IF}$

Multistage decimation is the preferred architecture for most applications. In our receiver, decimation is achieved in stages of 2 – 2 – 2 (F_s=160MHz, B=20MHz). The first stage contains two halfband real filters (AAF1) applied to I/Q bitstreams coming from the CT ΔΣ modulator. The complex filtering is achieved in the next stage (IR1&IR2) to perform image rejection and to generate the real two sided band desired signal. The two last decimation filters (AAF2 & AAF3) are placed at the end of the decimation chain to achieve channel selection.

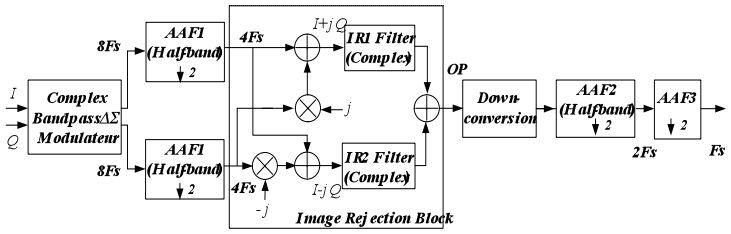

Figure 2. Block Diagram of Decimation Structure

Furthermore, we need frequency down-conversion as shown in Figure 2. A basic implementation of this scheme require two multipliers; for real and imaginary terms of the complex exponential $e^{-j\omega 0t}$. A careful choice of the sampling frequency yields a simplified implementation. If $\omega_0=\pi/2$ ($f_0/F_s=1/4$), the sine and cosine sequences have a simple structure: each term is either 0 or ±1. Thus, the sequence can be written as (1) for F_s = 80 MHz and $f_0 = F_{IF}$ = 20MHz.

$$\sin\left(2\pi\frac{f_0}{F_s}t\right)=\sin\left(\frac{\pi}{2}t\right)=\{0,1,0,-1,0,1,0,-1,...\} \quad (1)$$

B. Digital Image Reject Process

Now, we plan to remove the image signal and get the real signal from signals at $\pm F_{IF}$. This could be achieved by doing a complex filtering of the AAF1 filter outputs. The CT ΔΣ modulator has a complex NTF and STF (signal transfer function). A complex sum or difference of first decimation filter (AAF1) output has the following frequency components:

- The desired signal at $\pm F_{IF}$
- The image signal attenuated by the STF
- The quantization noise shaped according to the NTF

These components are shown in Figure 3. The complex STF pass the desired signal and attenuates the image signal partially from the complex outputs sum and difference. The complex NTF shapes the quantization noise. The digital filters need to attenuate the image signal and the quantization noise present outside the signal band. The transfer functions of the two complex digital filters IR1 et IR2 are given in (2) and (3).

$$H_{IR1}(z)=H_{RE}(z)-j*H_{IM}(z) \quad (2)$$

$$H_{IR2}(z)=H_{RE}(z)+j*H_{IM}(z) \quad (3)$$

where H_{RE} and H_{IM} are real transfer functions.

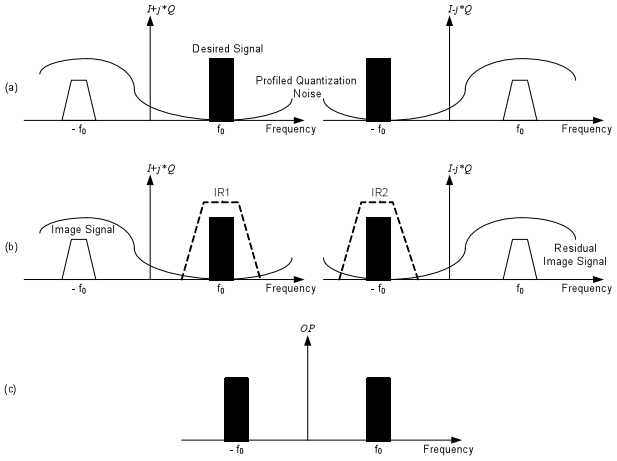

Figure 3. Down Conversion Stage Structure

From these expressions, the complex image rejection filters have complex conjugate transfer functions pair. The computational complexity can be drastically reduced by doing a simple mathematical operation, as shown in (4):

$$OP = [I + j*Q][H_{RE} - j*H_{IM})] + [I - j*Q][H_{RE} + j*H_{IM})]$$
$$OP = 2.[I*H_{RE} + Q*H_{IM}] \quad (4)$$

In fact, it is obvious that complex digital filtering can be accomplished by using two real filters corresponding to the real and the imaginary parts of IR1/IR2 transfer function. This structure is shown in Figure 4. This optimization reduces the computational complexity to one fourth.

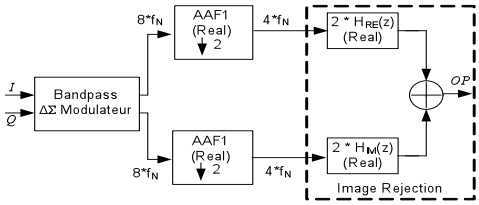

Figure 4. Optimized Image Rejection Block

C. Simulation Results

The signal and noise components present in the CT ΔΣ modulator output data is now analyzed. Figure 5 shows the spectrum of the complex sum of the modulator output bit streams ($I+jQ$) for a single tone. Here, $F_s=160MHz$, $F_{IF}=20MHz$.

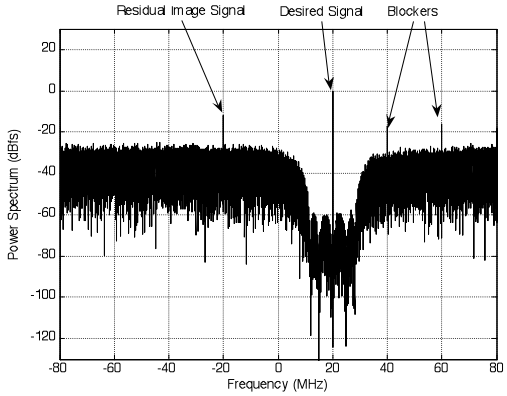

Figure 5. Modulator Output Spectrum

Table 3 shows filter specifications of different stages of decimation. The synthesis results from Matlab are also summed up in table 3. A first system level validation is done under Simulink software.

Filter	AAF1	IR1	IR2	AAF2	AAF3
Type	Real	Complex	Complex	Real	Real
Structure	Half-band	FIR	FIR	Half-band	FIR
Sampling frequency f_S (MHz)	160	80	80	80	40
Decimation factor	2	-	-	2	2
Band pass frequency f_{pass} (MHz)	30	[10, 30]	[-30, -10]	12	6
Cutoff frequency f_{stop} (MHz)	40	-	-	20	8
Stop band Rejection (dB)	45	50	50	65	45
Order	18	22	22	14	18

Table 3. Filter specifications

V. Implementation Results

All the filters are implemented with direct form structures, using two's complement arithmetic. The Signal to Noise Ratio (SNR) was computed at each stage of the filter chain with number of bits for data quantization being varied. The optimum bit allocation is as follows: 13 bits for the filter coefficients and 14 bits for the filter input. Figures 6 and 7 illustrate, respectively, the spectrum analysis of complex sum of AAF1 outputs and the spectrum analysis of real output of image rejection block at IF.

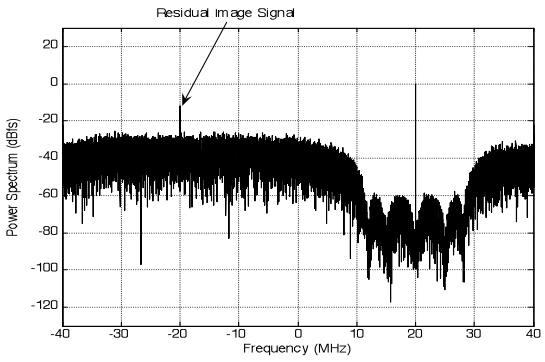

Figure 6. AAF1 Output Spectrum

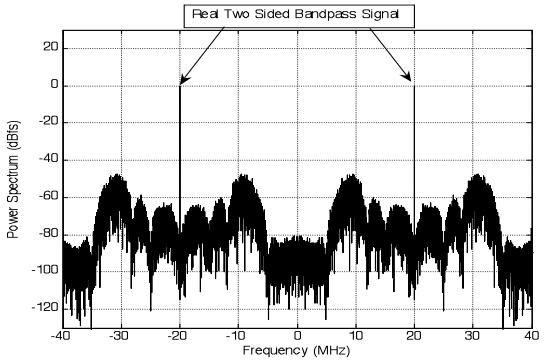

Figure 7. Image Rejection Block Output Spectrum

Figures 8 and 9 show, respectively, the spectrum analysis of down conversion output and the spectrum analysis of final decimation chain output.

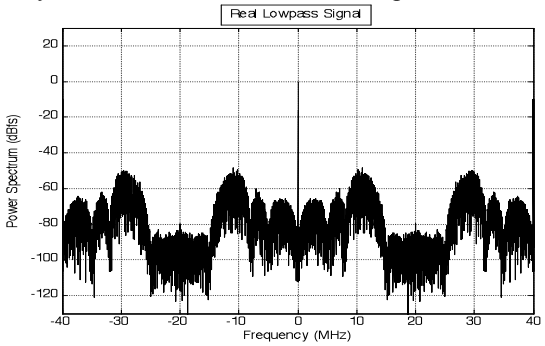

Figure 8. Down Conversion Output Spectrum

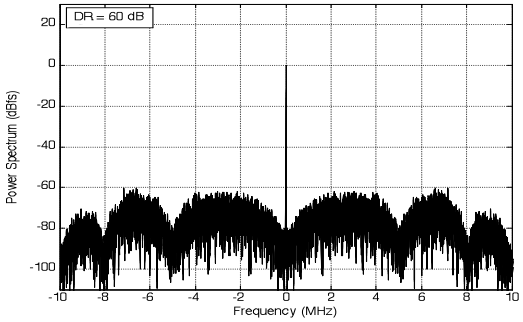

Figure 9. Hole decimation chain Output Spectrum

As we can see, the full dynamic range of the receiver is respected (DRADC), and the digital decimation filter guarantee the required processing. Various architectures were evaluated as function of area and power optimization. The first optimization method is a structural one: decimation filters are implemented over polyphase architecture. Linear phase decimation filters have a symmetric impulse response, then the polyphase subfilter's coefficients are symmetric or mirror image pairs. These symmetries can be used in efficient calculation structures that give an additional reduction factor by two in the multiplication rates [6]. The second optimization method is based on coding all coefficients of decimation and image reject filters with canonical signed digits (CSD). Then, filter's coefficients are implemented with only shift and add stages. In order to validate our decimation structure on low-cost digital CMOS process, we choose SPARTAN 3E family for implementation. The chosen component, xc3s500e-5fg320, is with 90nm digital CMOS process. The table 4 resumes implementation and experimental results for each filter. Two configurations are tested and compared for all filters: direct

form using multipliers and polyphase form using CSD coded coefficients. We note that only by using proposed optimized techniques, AAF1 filter satisfy the specifications with working frequency more than the required frequency (160 MHz). The same remark is true for IRRE and IRIM filter working at 80 MHz. By using circuit's level optimization, the second decimation filter AAF2 satisfies the specification (80 MHz).

		FPGA Resources			
	Implementation Structure	Logic cells	Flip Flop	LUT	f_{max}
AAF1	Polyphase Form CSD Coded Coefficients	82 127	58 146	80 211	74.223MHz 168.388MHz
IR_{RE}	Direct Form CSD Coded Coefficients	320 443	336 390	275 710	67.550MHz 88.637MHz
IR_{IM}	Direct Form CSD Coded Coefficients	279 368	322 354	203 577	64.584MHz 88.069MHz
Down-Conversion	$F_0 / F_s = \pi/2$	24	17	45	284.904MHz
AAF2	Polyphase Form CSD Coded Coefficients	158 214	180 197	144 387	75.682MHz 83.611MHz
AAF3	Direct Form CSD Coded Coefficients	313 462	306 358	354 791	64.516MHz 78.912MHz

Table 4. Implementation Results

VI. Conclusions

In this paper, optimized decimation filter architecture for low IF Receiver using complex bandpass ΔΣ modulator is presented. The digital filter performs channel selection, complex wideband filtering at IF to reject image signal and converts the ADC output from complex signal to a real signal, sampled at a rate equal to one-eighth of the sample rate of the ADC. Attention was focused on the decimation chain partition, optimization and implementation of the channel selection filtering and image rejection block. Thus, we fulfill all the receiver constraints especially the dynamic range. The achieved high speed and the low complexity of this decimator, when implemented in Spartan FPGA, make it very appropriate for the implementation of the decimation path of a Low-IF receiver. Future work will take care of more accurate characterization based on other circuit optimization methods to achieve the most important constraint, the working frequency.

References

[1] A. A. Abidi, "The Path to the Software-Defined Radio Receiver", IEEE Journal of Solid-State Circuits, vol 42, Issue 5, pp. 954 - 966, May 2007.

[2] N. Jouida, C. Rebai, A. Ghazel and D. Dallet, "Comparative Study between Continuous-Time Real and Quadrature Bandpass Delta Sigma Modulator for Multistandard Radio Receiver", IEEE IMTC'2007, Warsaw, Poland, May 1-3, 2007.

[3] L. Breems, and J.H. Huijsing, "Continuous-Time Sigma-Delta Modulation for A/D Conversion in Radio Receivers," *Kluwer Academic Publisher*, Boston, 2001.

[4] J. Crols and M.S.J. Steyaert, "Low-IF topologies for high-performance analog front ends of fullyintegrated receivers", *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, Vol 45, Issue 3, pp. 269 - 282, Mar 1998.

[5] B. A. White and M. I. Elmasry, "Wireless transceiver architecture: Digital IF receiver," Tech. Rep., VLSI Research Group, Univ.Waterloo,Waterloo, Canada, Apr. 1999.

[6] N. Jouida, C. Rebai, A. Ghazel and D. Dallet, "Built-in Filtering for Out-of-Channel Interferers in Continuous-Time Quadrature Bandpass Delta Sigma Modulators" *IEEE ICECS*, Marrakech, Morroco, 11-14 Dec. 2007.

[7] ''Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications: High-Speed Physical Layer in the 5 GHz Band'', IEEE Std 802.11a-1999.

[8] ''Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications International Standard'', IEEE Std 802.16-2000.

[9] N. Jouida, C. Rebai, A. Ghazel, D. Dallet, "Continuous-Time Complex Bandpass ΣΔ Modulator: Key Component for Highly Digitized Receiver," IEEE ICECS, Nice, France, 10-13 Dec. 2006.