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A simplified 3 –bits discrete pure linear analog preprocessing folding ADC architecture

Fabio Leccese

Electronic Engineering Department, University of Roma "Roma Tre"
Via della Vasca Navale n.84 00146, Roma, Italy, tel. 06 57337085, fax. 06 57337101,
leccese@uniroma3.it

Abstract- A simplified architecture of subranging pure linear folding ADC is proposed. The device is based on the folding idea to eliminate the DAC, the summing node and the amplifier, fundamental elements of the classical architecture, replacing them by means of an analogical signal preprocessing parallel structure named "channels". The presented circuit in addition to the advantage of a reduction of total conversion time than a classical subranging ADC, so approaching ADC flashes, is very simple and easy to build. An accurate simulation of the single channels and of the whole structure validate the idea. A first discrete circuit it has been realized and tested.

I. Introduction

With the constant growth of digital systems and digital processing techniques, the demand of analog to digital converters (ADC) is rapidly increasing. The ADC have been developed using a number of different architectures suitable for different applications and able to satisfy different necessities linked to resolution, speed and power consumption[1]. In the field of very high speed, the flash ADC remains dominant. For these, the 2^N-1 reference voltages, obtained by a thermometric resistor ladder, are directly compared with the input voltage by 2^N-1 comparators. Their binary output is encoded by a diode encoder which output gives a N-bit digital word. So the N-bit digital word represents the input voltage relative to the reference voltages of the reference ladder. The structural limit of the flash ADC is joined to its resolution; in fact the internal elements, and their inherent typical problems, exponentially increases with resolution. So the maximum resolution is not more than 10-bits.
For applications which high speed and high resolution are contemporaneously required, the subranging structures gradually replaced flash ADC's. This kind of architecture achieves high resolution and conversion accuracy with fewer elements than flash ADC one, which, however, is at the expense of the speed and bandwith[2,3].
The folding is a version of the subranging architecture. By means of an analog preprocessing circuit in folding A/D converters the number of comparators can be reduced significantly. Folding architecture reduces the total conversion time than a classical subranging ADC almost achieving the flash one even if the power consumption is quite high[1].
In this paper, a simplified linear folding architecture for subranging ADC is presented. The preprocessing analog structure is constituted with 2^n (with n number of bits) parallel circuits made with a simple subtracting node and with a series of two mos switches able to join the functionalities of DAC, summing node and amplifier typical of classical subranging ADC. To validate the idea, after accurate simulation of the singles channels and of the whole structure, a first discrete circuit it has been realized and tested.

II. Classic subranging and linear folding ADC

The main motivation of the introduction of the subranging A/D converter is the elevated reduction of the number of comparators required in the design than a full flash ADC. For this architecture there are two principal implementations: the two-steps and the folding[4].
The two-steps A/D converter gets efficiency by dividing an *N*-bits quantization into lower-resolution quantization. In such a converter the first n_1-bits quantizer called "coarse" digitizes the input signal with low resolution, and applies the resultant codeword to the reconstruction DAC. The analog output of the DAC is subtracted from the original input to form a residue signal, which is quantized by an n_2-bits quantizer. The advantage of this approach arises because the combined complexity of the n_1-bit coarse and the n_2-bit fine quantizers can be far less than the complexity of a single *N*-bits quantizer.

The target of a folding A/D converter is to form the residue signal with simple analog circuits thereby obviating the need for the coarse quantizer, the DAC, and the subtracter of subranging ADC. In such an implementation (figure 1a), the low dynamic-range residue signal generated by the analog folding circuit directly drives the fine quantizer. Because of the periodic nature the residual signal; however, the digitized output from the fine quantizer is ambiguous, and coarse quantizer is still necessary to ascertain in which period of the folding circuits transfer characteristic the quantizer input signal lies. The input-output characteristic of the analog folding circuit can be parameterized by the number of piece-wise linear segments, of folds, which it contains. The idea of folding is similar to a two-steps ADC: both structures utilize two lower resolution quantizers to implement one higher resolution ADC. However, folding ADCs use analog preprocessing to generate "residue" at the same instant that the MSBs are produced from the coarse quantizer. Also the coarse quantizer determines where the input lies for the folding amplifier (analog preprocessing). The total resolution of the folding ADC is $N_B = n_{MSB} + n_{LSB}$, where n_{MSB} and n_{LSB} are the numbers of bits resolved in the coarse and fine quantizers, respectively.

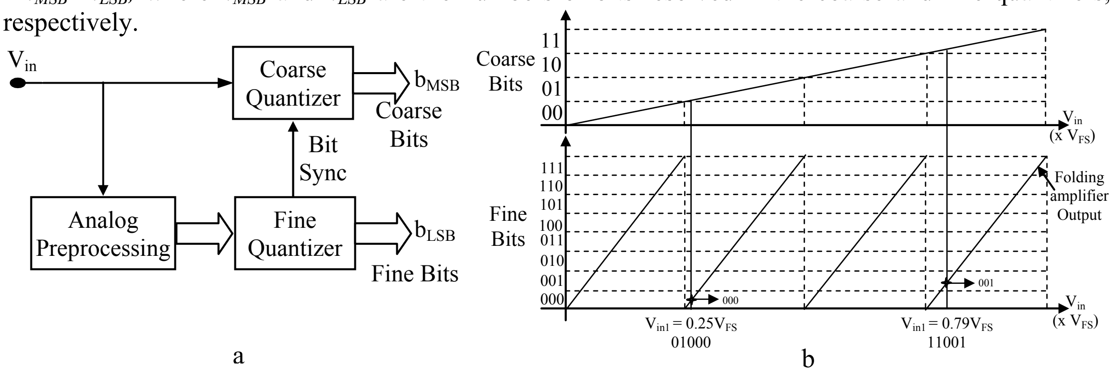


Figure1. A 5-bit example: 2 coarse bits plus 3 fine bits (a) block diagram (b) generation of coarse and fine bits.

A 5-bit ADC (figure 1) is used as an example to explain the basic idea of folding ADCs. The output (figure 1b) repeated four times when the input voltage sweeps through the full ADC range. Thus a comparator in a folding ADC will detect four zero crossing points while a comparator in the flash ADC will detect only one. In this 5-bit folding ADC, a total of 10 (3 for coarse and 7 for fine quantizer) comparators are needed while a 5-bit full-flash ADC needs 31 comparators. Generally speaking, a folding ADC reuses comparators so that the total number of comparators can be reduced by a folding factor (F_F), i.e., 4 in figure 1.

III. The classic analog preprocessing circuit

In the previous folding architecture the analog preprocessing segments represent the most important part of the circuit because both the coarse and fine quantizer are full flash ADC. There are several methods to realize this circuits. The basic configuration is based on diode[5], very simple to realize but suffers in case of large input swing requirement. Another configuration is based on current-mirror that can be used to implement piecewise linear transfer characteristic of folding amplifier. The cascade current mirror version is strongly suitable for low voltage low power design, but, to obtain adequate accuracy, the length of transistor have to be large with disadvantage of low speed[6]. Another technique uses folding amplifier based on hyperbolic tangent transfer function of voltage differential pairs. This scheme solve bandwidth problem, but it suffers of intrinsic output current distortion that limits the number of folds[7]. Some of these drawbacks are overcome by wired-OR configuration at the differential pair outputs to reduce the common-mode output signal and to provide buffering, but this circuit still suffers from the threshold perturbing effects of a single-ended reference scheme[8].

IV. The circuit proposed

After the sample-and-hold the signal is sent to a structure made with 2^N channels that realize the analog preprocessing signal. The channels are divided in two parts: the first realizes the subtraction between the sampled input signal and reference voltage, while the second transfers the remaining analog voltage to the second ADC flash by means of electronic switches. The block scheme is proposed in figure 2 ($V_{quantum}$ = 0.625V). Each channel is activated in correspondence of a pre-fixed voltage limit individualized by the analogical voltage associable to the n^{th} quantum. They are able to subtract to the sampled input signal a voltage corresponding to (n-1)th quantum so that the value of the remaining analog voltage is inclusive in the single quantum. The subtracter output signal is able to activate the switches only if it is included in the $V_{quantum}$ range so, when a channel is activated, the others are mutually left out. The subtracter is obtained by means of a simple operational amplifier in differential configuration. The capacitor of Sample/Hold is directly connected on "non inverting" input. On "inverting" input is connected a JFET current generator able to produce a constant current. Varying feedback resistors will be possible obtain the wanted voltage reference to subtract to the S/H voltage. In this way it is possible to join the buffer function of the second AMP-OP of the S/H with the channel subtracter function. The switches are based on MOS technology. When the voltage rises the first switch of the generic channel will be normally opened, while the second normally closed. Only the first channel has only a normally closed switch. These switches are driven by the same signal that they have to send to the fine quantizer. A normally closed switch is in the ON state until its input value is lower than a fixed limit, while a normally opened switch is in the OFF state for input values lower than fixed limit. The series of these two switches realizes a window able to transfer the input voltage only if it is included between the fixed limits. The channel circuit is shown in figure 3. The output subtracter signal is sent on the source of a NMOS which body is connected to -5 V to maintain inversely polarized the p-n junction between body and source and between body and drain. The drain of the NMOS is the output of the channel and it is picked up on a resistor with a value much higher than R_{ON} of the NMOS. The NMOS switch is driven by another MOSFET that acts on its gate. The command is a bi-state signal able to maintain the NMOS or in linear region or in cut-off one. The command signal will be equal to +5 V only if the subtracter output is included in the $V_{quantum}$. Using a ramp input signal it is easy to obtain a step output that starts at 5 V and arrives to 0 V by means of a NMOS switch (figure 4a). V_{GATE} is the input voltage coming from subtracter; on the drain is placed a resistor with the second pole on +5 V, while on the source there is a constant voltage. This configuration allows to the NMOS to give +5 V on drain until the V_{GS} is smaller than V_{TH} while it gives the V_S when V_{GS} is larger than V_{TH}. By the V_S is possible to fix the input value that allows the control of the MOS switch. This value is the sum of V_{TH} and V_S. Figure 4b shows the input ramp signal and the step output.

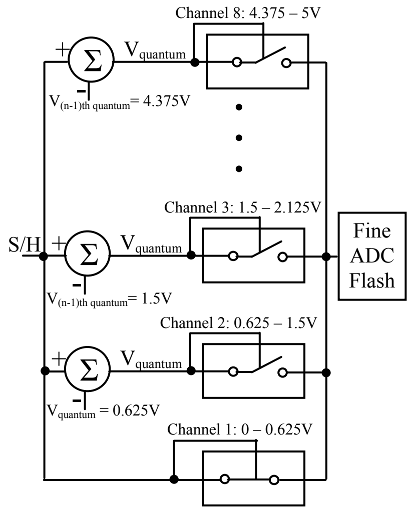


Figure2. Analog preprocessing circuit scheme block

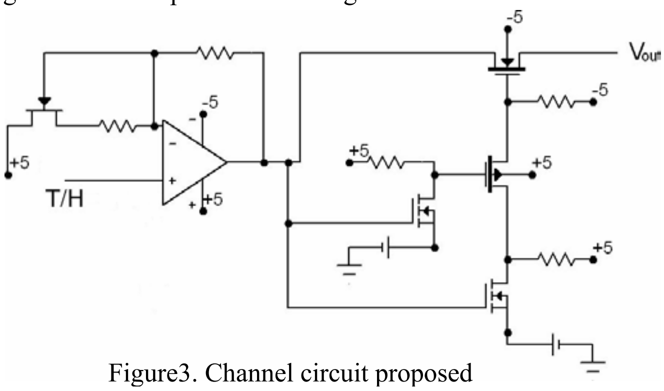
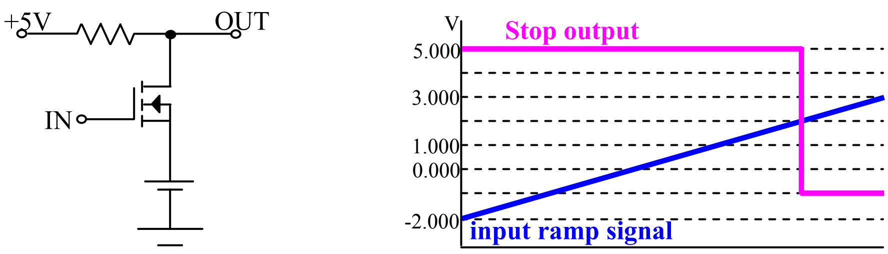


Figure3. Channel circuit proposed



a) b)

Figure4. a) NMOS switch b) input ramp signal and step output

Now it is necessary to select the part of signal higher than a fixed limit. To obtain it, it is possible to send the step signal on a PMOS piloted in such a way to cut the unwanted part. The pilot signal will be again a step signal that passes from 0 to 5V in function of the ramp growth. The circuit is shown in figure 5a.

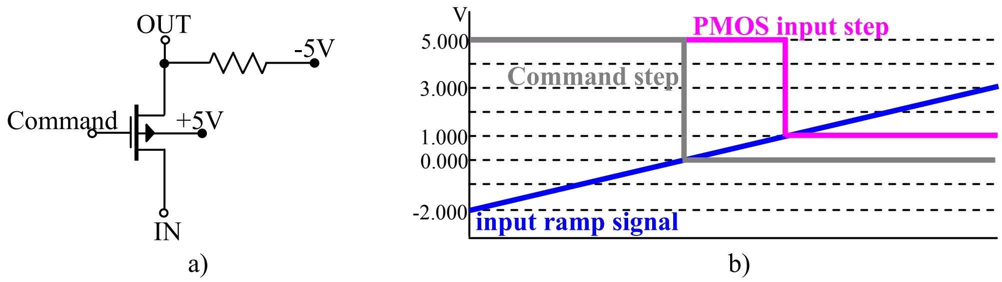


Figure5. a) PMOS switch b) command step, PMOS input step and ramp subtracter output.

The input is on the source, the output on the drain and pilot signal on the gate. In this case, to maintain the p-n junction in inverse polarization, it is necessary to put the body to +5V. The output of the PMOS have to follow the input so it is necessary to put on the gate a voltage that bring the V_{GS} lower than V_{TH}; instead, to avoid that the input passes on the drain, it is necessary to have on the PMOS gate a voltage able to bring the V_{GS} higher than V_{TH}. The signal will be high for negative subtracter output value, low otherwise. Figure 5b shows the graph of the two steps: the command step and the PMOS input step close to the ramp subtracter output. As it is possible to see from the PMOS circuit, on the output drain is placed a resistor with a pole placed to negative voltage -5V; this is necessary to obtain a -5 V low voltage that permits to impose the cut-off to the NMOS. Connected the two NMOS switches that generate the ramps and the PMOS, the NMOS switch pilot circuit is realized. It is able to close the switch only for source input values included between two arbitrarily fixed limits. In the next graphs are shown the final NMOS switch pilot signal in function of the ramp subtracter output (figure 6a) and the NMOS output with its input signal (figure 6b). The whole circuit is composed by eight channels connected on a single resistor much higher than R_{ON} of the NMOS. This simplicity is due to the fact that only one channel is activated so, applying the Thevenin principle, the output resistor see always a NMOS in linear region and seven open circuit. Figure 6c shows the output of generic channel in the whole circuit.

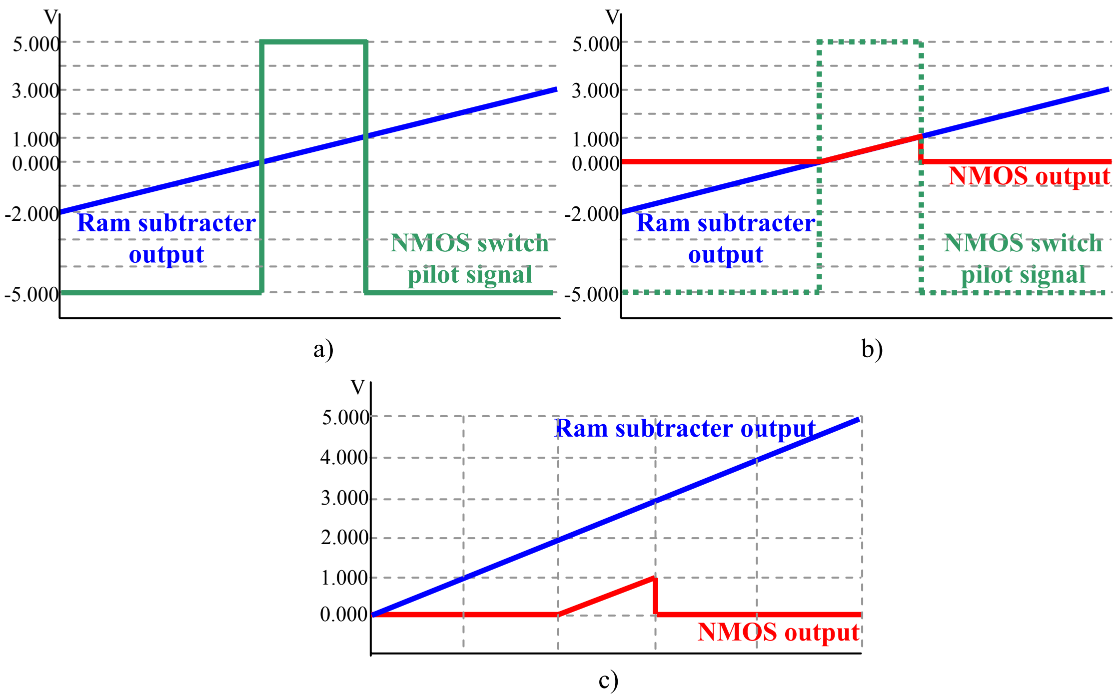
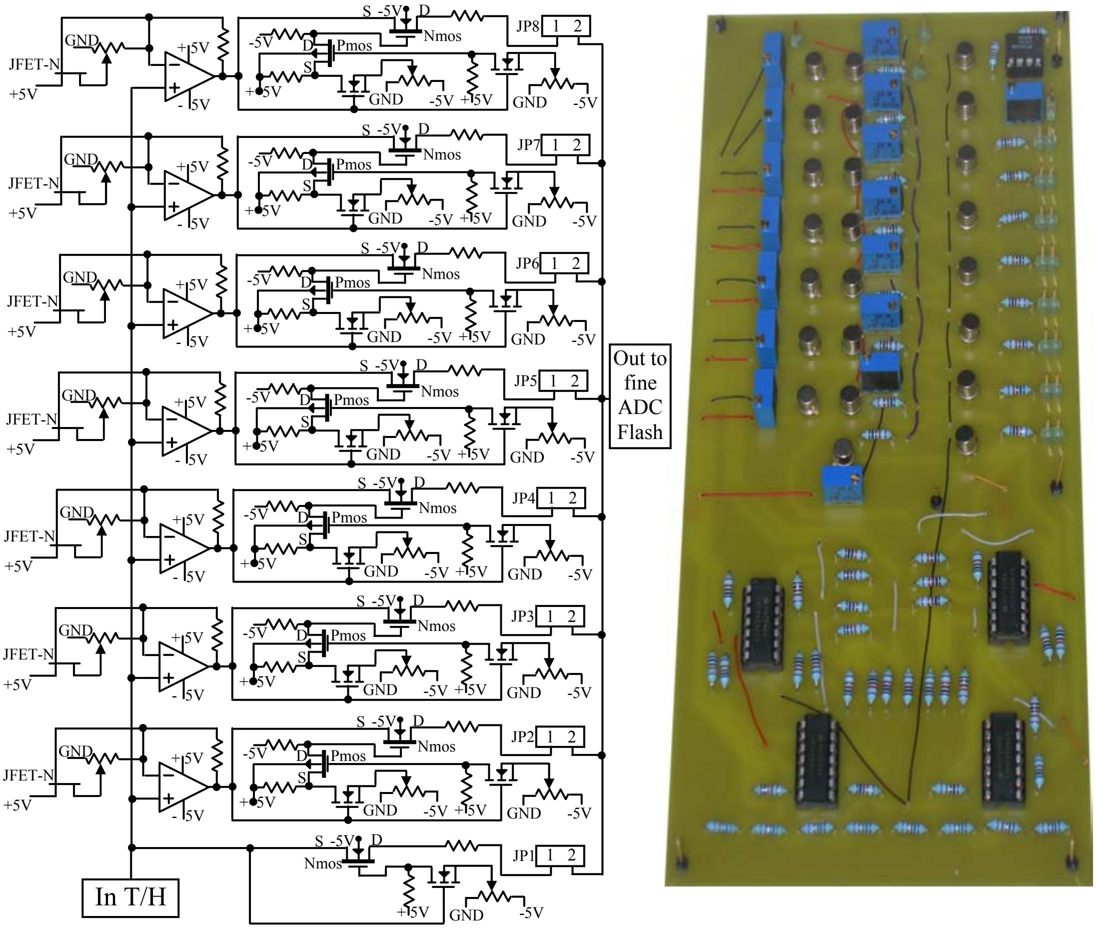


Figure6. a) final NMOS switch pilot signal b) NMOS output c) total circuit output.

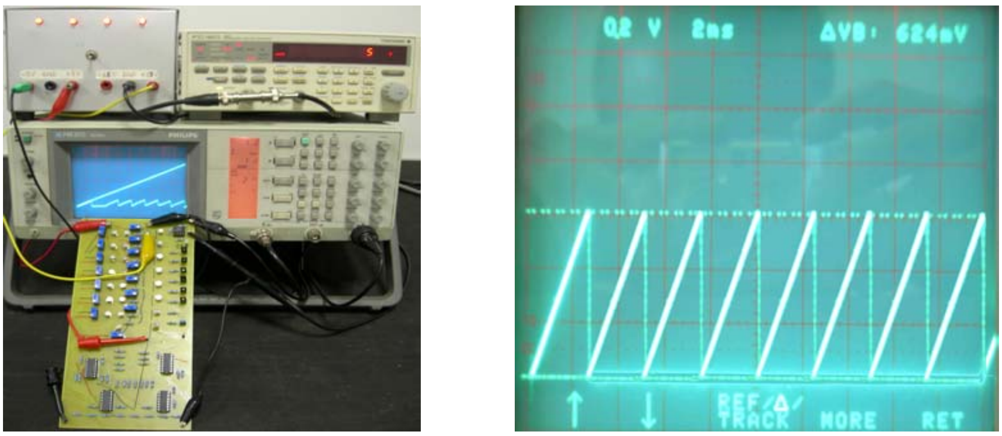
V. The experimental results

The circuit has been realized with discrete component. For the NMOS switch, we used the Calogic enhancement NMOS transistor IT1750 that have the body separated by the source, with values for $V_{GS(th)}$ included between 0.5 and 3 V, a $r_{DS(ON)}$ of 50 Ω and an I_{DSS} of 10 nA. Figure 6a shows the schematic, figure 6b shows the realized circuit, figure 7a shows the measurement bench with a stabilized energy supplier, a Philips PM3070 oscilloscope and a Yokogawa FG120 function generator and 7b shows the oscilloscope output circuit signal when the input is a ramp function between 0 and 5 V.



a) b)

Figure6. a) Schematic circuit b) Discrete PCB circuit.



a) b)

Figure7. a) Measurement bench b) Oscilloscope test.

The last two figures show as the circuit realizes the pure linear folding transfer function. On the oscilloscope it is possible to read a voltage quantum of 624 mV because the its resolution is 2 mV. The maximum resolution obtainable by this circuit with the Calogic's components is 78.125 mV equal to a possible discrete pure linear analog preprocessing folding of 64 channels so to conceive a possible folding ADC with 12 bits resolution, the six MSBs managed by a 6-bits coarse ADC flash and the lasts six bits managed by the folding architecture.

VI. Conclusions

A simplified architecture of a 3-bit discrete subranging pure linear folding ADC has been proposed. Accurate simulations of the circuit validate the idea. A first discrete circuit it has been realized and tested.
To talk of conclusions is too early, this is an “in itinere” work so it is preferable to talk of future perspectives. The next steps of this work will be to improve the resolution establishing the higher resolution limit with discrete MOS evaluating MOS of other producers, after that it will be necessary to evaluate the possible conversion errors joined with this structure mainly analyzing the synchronism between the two ADCs flash. The bandwidth of the circuit should be evaluated, but it should be preferable to face this last step with an integrated circuit.

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