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Modelling and Simulation Analysis of Intelligent Pipeline A/D Converters[1]

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Abstract **-** The paper is devoted to the methods of analysis of a new class of “intelligent” pipeline A/D converters (IP ADC). The conversion scheme used in IP ADC is based on the original analytically grounded approach to optimisation of adaptive estimation systems. Its application to the pipeline A/D converters design leads to changes in the architecture and principles of conversion in comparison to solutions used in conventional pipeline A/D converters. The paper focuses on modelling and analysis of dependence of IP ADC performance on the parameters of their analogue components and conversion algorithm. The main goal was to develop appropriate methods and simulation tools which enable effective assessment of the close to optimal parameters of IP ADC components before the realization of its hardware prototype. The results of selected simulation experiments related to analysis of influence of parameters of analogue and digital components on final performance of IP ADC are presented and discussed in the paper.

I. Introduction

Intelligent pipeline A/D converters (IP ADC) employ the new pipeline A/D conversion method and the corresponding architecture, which is the consequence of application of the analytical approach [1] to optimisation of adaptive estimation algorithms. The approach permits to determine analytically the most efficient, under given conditions, structure and values of converter parameters which guarantee maximal performance of conversion under given permissible probability of saturation. The approach was applied earlier to optimisation and design of intelligent cyclic A/D converters (IC ADC) [2-3]. The laboratory prototype of IC ADC realized in CMOS AMS 0.35 μm technology is now investigated.

Application of the approach to pipeline A/D converters (PADC) design leads to changes in the architecture and principles of pipeline A/D conversion. The most important one is resignation from the common for conventional PADC method of the codes computing based on the shifting and summarizing low-bit binary words delivered by sequential stages of PADC [4-5]. In IP ADC, these codes are computed in each stage of conversion as long-bit binary words of fixed length N_{comp} (N_{comp} = 12÷32-bits depending on required resolution of IP ADC). This creates a possibility to compute the codes using the adaptive estimation algorithms proposed in [1]. Transition to the long-bit operations in IP ADC permits to remove inevitable in known pipeline ADC constraints on the gain coefficients in sequential stages of the converter, i.e. gains should have only the values equal to integer powers of two. Impossibility to set the gains to each theoretically required value restricts possibilities to utilize entirely the resources of the analogue components of PADC for reduction of influence of technological errors and noises. On the other hand, to avoid overloading in particular stages, designers artificially decrease the gains of amplifiers. The latter results in incomplete utilization of the resources of converter components and decreases its final resolution. In IP ADC, potential overloading is excluded by setting the components parameters in each stage to the close to optimal values determined analytically or in simulation experiments at the initial stage of the design process.

General principles of IP ADC functioning were presented and discussed in [6], where the potential possibility of performance improvement of one of existing pipeline A/D converters (AD9240) using the proposed conversion scheme was shown. The main goal of investigations, which results are presented in this paper, was to develop appropriate methods and simulation tools for IP ADC performance assessment and analysis. The proposed methods and simulation tools enable effective assessment of required parameters of IP ADC components at the initial stage of IP ADC design.

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II. Intelligent Pipeline ADC versus Conventional Pipeline ADC

A simplified architecture of a conventional pipeline A/D converter is shown in Fig. 1 [4-5] (compare e.g. AD9240 or AD6645 [7]). PADC consists of *K* stages and a digital correction logic block. Each *k*-th ($k = 1, 2, ..., K$) stage of the converter provides, on the basis of its input signal $e_{k-1}^{(n-k+1)}$, the binary code $\hat{q}_k^{(n-k)}$ and the residual output signal $e_k^{(n-k)}$, which is routed to the next (*k*+1)-th stage. Each stage of the conventional PADC consists of the sample and hold block (S/H), the internal low resolution flash A/D converter (sub-A/D converter - SADC$_k$) connected to the internal D/A converter (sub-D/A converter - SDAC$_k$), the analogue subtractor (Σ) and the amplifier with the gain G_k. The last stage consists of S/H block and the internal flash A/D converter (SADC$_K$). The internal SADC$_k$ forms the binary code $\hat{q}_k^{(n-k)}$ of the input residual signal $e_{k-1}^{(n-k+1)}$ directed to the digital correction logic block. Simultaneously, SDAC$_k$ forms the analogue equivalent $\hat{e}_{k-1}^{(n-k+1)}$ of the code $\hat{q}_k^{(n-k)}$, and the difference between the input residual signal $e_{k-1}^{(n-k+1)}$ and the analogue equivalent of the code $\hat{q}_k^{(n-k)}$ at the SDAC$_k$ output is amplified G_k times in the amplifier. The amplified signal $e_k^{(n-k)} = G_k(e_{k-1}^{(n-k+1)} - \hat{e}_{k-1}^{(n-k+1)})$ is routed to the next (*k*+1)-th stage. All the codes $\hat{q}_k^{(n-k)}$ are collected in the digital correction logic block, where they are combined and the digital output data is produced.

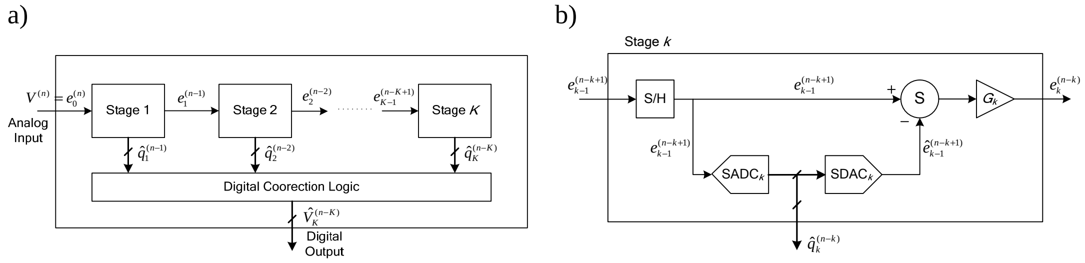

Figure 1. Architectures of conventional pipeline A/D converter (a) and its *k*-th stage (b).

In known converters, the gain coefficients G_k may have only the values equal to the appropriate powers of two $G_k = 2^{M_k - m_k}$, where M_k (1÷6 bits) is the number of bits of the internal coarse A/D converters SADC$_k$ (M_k = 1÷6 bits), and m_k is the number of redundant bits used for digital correction of the errors caused in the previous stage. Usually, in actual pipeline converters [7], one bit of redundancy is used, that is $m_k = 1$. Introduction of additional redundant (overlap) bit(s) and corresponding decrease of the gain G_k is done in order to avoid possible rough errors of the particular stages overloading [4], which causes that missing codes appear in the overall transfer function of the pipeline A/D converter without redundant bits. Decrease of the gain G_k, as it was said above, diminishes potentially achievable resolution of PADC.

Also analytical quantitative assessment of the probability of the PADC stages overloading is a very complex task. This is the result of immanent nonlinearities of sub-converters SADC$_k$ and SDAC$_k$ as well as analogue noises of amplifiers, subtractors and S/H units.

The architecture of the proposed IP ADC is presented in Fig. 2. Each stage of IP ADC (see Fig. 2b) includes a sample and hold block (S/H), which holds the constant voltage $V^{(n-k+1)} = V$ (for notational convenience, the upper time index is further omitted) at the input of an analogue subtractor (Σ$_1$). This voltage V is transferred unchanged from the previous stage to the next one until it reaches the final stage in the converter. In each *k*-th stage, a new value of the input sample code (estimate) $\hat{V}_k^{(n-k)}$ is calculated on the basis of the value of the voltage V and its digital code $\hat{V}_{k-1}^{(n-k+1)}$ calculated in the previous (*k*-1)-th stage of IP ADC.

The second (negative) input of the subtracor Σ$_1$ is connected to the output of an internal sub-D/A converter (SDAC$_k$). SDAC$_k$ forms the analogue value $\hat{V}_{k-1}^{DAC}$ of the binary $N_{DAC,k}$-bit code ($N_{DAC,k} < N_{comp}$) of the estimate $\hat{V}_{k-1}$ calculated in the previous stage according to the formula:

$$\hat{V}_k = \hat{V}_{k-1} + L_k \tilde{y}_k \, . \tag{1}$$

The residual signal $e_k = V - \hat{V}_{k-1}^{DAC} + \nu_k$ at the output of Σ$_1$ is routed to the input of the amplifier (A) with the gain *C*$_k$. The amplified signal $C_k e_k$ is routed to the input of the internal coarse ($N_{ADC,k}$ = 1÷6 bits) sub-A/D converter SADC$_k$. $N_{ADC,k}$-bit code $\tilde{y}_k = C_k e_k + \xi_k$ formed by SADC$_k$ is routed to the digital part of the stage. Variables ν_k and ξ_k in above expressions for residuals and observations represent the analogue and quantisation noises, respectively.

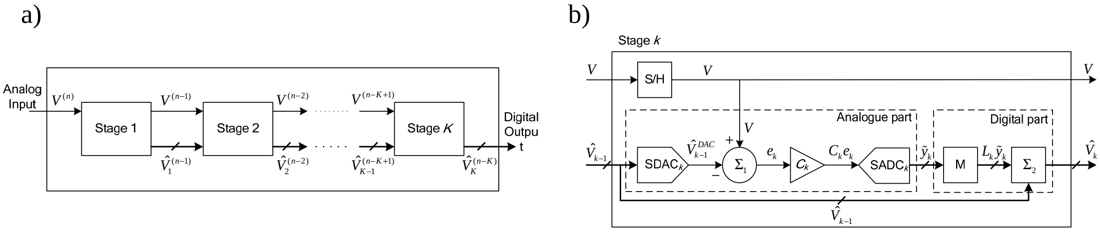

Figure 2. Simplified architectures of the proposed IP ADC (a) and its *k*-th stage (b).

Optimal values of the gains C_k (maximal under given acceptable probability of overloading μ) as well as corresponding values of coefficients L_k can be found using the analytical approach proposed in [1]:

$$C_k = \frac{D_{ADC,k}}{\alpha\sqrt{\sigma_{\nu,k}^2 + P_{k-1}}}, \tag{2}$$

$$L_k = \frac{C_k P_k}{\sigma_{\xi,k}^2 + C_k^2 \sigma_{\nu,k}^2} = C_k^{-1}\left(1 - \frac{P_k}{P_{k-1}}\right). \tag{3}$$

These values minimize, for each $k = 1, 2, ..., K$, the mean square error (MSE) of conversion:

$$P_k = E[(\hat{V}_k - V)^2] = \frac{(\sigma_{\xi,k}^2 + C_k^2 \sigma_{\nu,k}^2) P_{k-1}}{\sigma_{\xi,k}^2 + C_k^2(\sigma_{\nu,k}^2 + P_{k-1})} = \left\{1 + \frac{C_k^2 P_{k-1}}{\sigma_{\xi,k}^2 + C_k^2 \sigma_{\nu,k}^2}\right\}^{-1} P_{k-1}, \tag{4}$$

under probability of overloading not greater than a given acceptable value μ. α in (2) is determined by the permissible probability μ of overloading of each stage, and in Gaussian case satisfies the equation

$$\Phi(\alpha) = \frac{1}{\sqrt{2\pi}} \int_0^{\alpha} \exp\left(-\frac{x^2}{2}\right) dx = \frac{1 - \mu}{2}. \tag{5}$$

On the basis of MSE of conversion (4), one can calculate effective number of bits (ENOB) of IP ADC using the following formula [8]:

$$N_k = \frac{1}{2}\log_2\left(\frac{P_0}{P_k}\right) = N_{k-1} + \frac{1}{2}\log_2\left(1 + \frac{C_k^2 P_{k-1}}{\sigma_{\xi,k}^2 + C_k^2 \sigma_{\nu,k}^2}\right), \tag{6}$$

which creates a possibility of analytical assessment of IP ADC performance depending on parameters of its internal components.

Non-Gaussian quantisation noise ξ_k makes the codes computed using the algorithm presented in [1] sub-optimal. This allows to develop the heuristic simulation and analytical methods which enable an increase of the gains C_k to the maximal permissible values and, in consequence, additional increase of IP ADC performance [8-9].

III. Modelling of IP ADC and Results of Experiments

MATLAB and SIMULINK models of intelligent pipeline ADC developed according to the diagrams presented in Fig. 2, were used for the assessment of requirements for IP ADC components and their influence on IP ADC performance. Fig. 3 shows the general structure of the SIMULINK models of IP ADC and its particular stage. Below, some results of investigations with the developed models are presented and discussed.

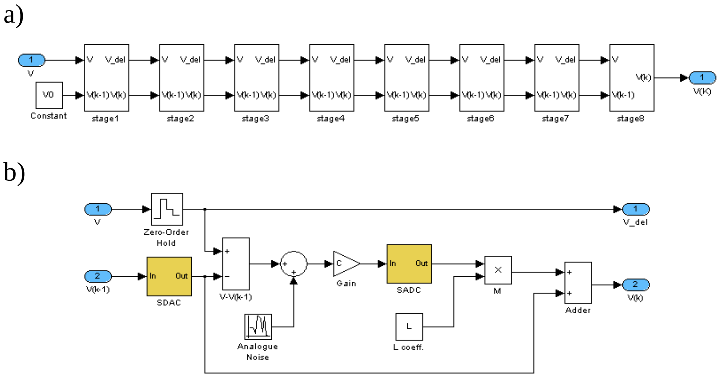

Figure 3. SIMULINK model of IP ADC (a) and its *k*-th stage (b).

In simulation experiments, test input signals were generated as sequences of sine-wave samples: $V^{(m)} = V_{\max} \sin(2\pi f_0 m)$, $(m = 1, \ldots, M)$, where $V_{\max}$ was taken equal to the half of full-scale range (FSR) of IP ADC and f_0 is the normalized frequency of the test signal. The values of parameters in simulations were as follows: $V_{\max} = 1$ [V], $f_0 = 409/8192$, $M = 8192$, $D_{DAC,k} = D_{DAC} = 1$ [V], $\mu = 10^{-4}$, $V_0 = 0$, $P_0 = FSR^2/12$. In simulations, standard measures of A/D converters performance [10] were used: root mean square error (RMS), effective number of bits (ENOB), signal to noise and distortion ratio (SINAD), and total harmonic distortion (THD). Empirical values of ENOB were calculated using the following formula:

$$\hat{N}_k = \frac{1}{2}\log_2\left(\frac{P_0}{\hat{P}_k}\right), \qquad RMS_k = \sqrt{\hat{P}_k} = \sqrt{\frac{1}{M}\sum_{m=1}^{M}[V^{(m)} - \hat{V}_k^{(m)}]^2}\,, \tag{7}$$

where *M* is the number of converted samples and empirical values of RMS of conversion were calculated according to the right formula in (7).

In IP ADC model, the modified versions of the relationships (2)-(3), based on “minimax” approach [8] to C_k optimization, were used:

$$C_k = \frac{D_{ADC,k}}{\Delta_{ADC,k-1}/(2 \cdot C_{k-1}) + \alpha\sqrt{\sigma_{\nu,k}^2 + \sigma_{\nu,k-1}^2} + \Delta_{DAC,k}/2}\,, \tag{8}$$

$$L_k = C_k^{-1}\,. \tag{9}$$

The idea of the minimax approach [8] consists in increasing C_k values to the maximal permissible values maintaining the “least favourable” signal at the input of each SADC$_k$ as close as possible to the boundaries of its FSR, but not exceeding these boundaries. Also, errors caused by the finite resolution of SDAC$_k$ were corrected. This was achieved using, instead of (1), the following formula [9]:

$$\hat{V}_k = \hat{V}_{k-1}^{DAC} + L_k \tilde{y}_k\,. \tag{10}$$

In the first series of experiments (Fig. 4), the expected values of ENOB of IP ADC for different resolutions ($N_{ADC,k} = 1, 2, 3, 4, 5, 6$ bits) of the sub-A/D converters were investigated. The experiments were performed under assumption that resolution of D/A sub-converters is $N_{DAC,k} = 10$ bit (Fig. 4a) and $N_{DAC,k} = 12$ bits (Fig. 4b). Simulations were performed without taking into consideration any nonidealities of IP ADC components apart from the limited resolution of internal sub-converters SADC$_k$ and SDAC$_k$. Plots in Fig. 4 show the maximal ENOB of IP ADC achievable under different resolutions of internal sub-converters and different numbers of IP ADC stages. For example, to achieve ENOB at a level of 15 bits for $N_{ADC,k} = 4$, $N_{DAC,k} = 12$, four stages in IP ADC structure are needed.

In the second series of experiments (Fig. 5), influence of the length N_{comp} of binary words $\hat{V}_k$, L_k, used in calculations in sequential stages of IP ADC, on the final performance of the converter was studied. The results, obtained for $N_{ADC,k} = 2$, $N_{DAC,k} = 10$ (Fig. 5a) and $N_{ADC,k} = 4$, $N_{DAC,k} = 12$ (Fig. 5b), show that the minimal length of the word which ensures that the computation errors (in the given conditions) do not worsen the obtained values of ENOB has the value $N_{comp} = 14$ (Fig. 5a) and $N_{comp} = 20$ bits (Fig. 5b), respectively.

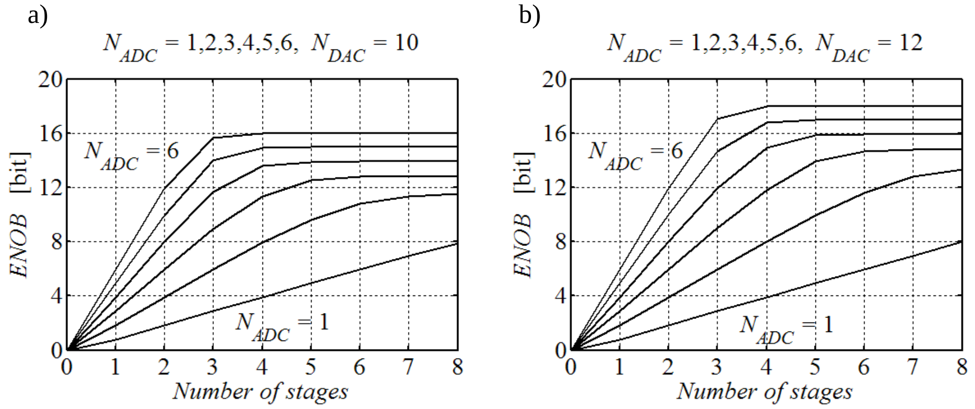

Figure 4. ENOB versus number of stages for different N_{ADC} under (a) $N_{DAC} = 10$, (b) $N_{DAC} = 12$.

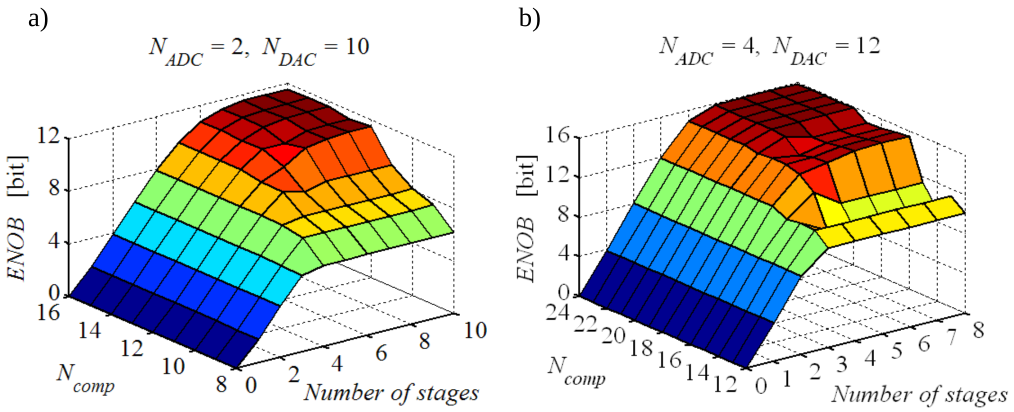

Figure 5. ENOB versus number of stages for different N_{comp} under (a) $N_{ADC} = 2$, $N_{DAC} = 10$, (b) $N_{ADC} = 4$, $N_{DAC} = 12$.

The third series of experiments (Fig. 6a) was devoted to the analysis of influence of internal analogue noises acting at the amplifier input (noises of subtractor, S/H, SDAC). The values of ENOB were assessed for different values of the root mean squares of analogue noises: σ_{an} from 0 to 10^{-4} [V]. The experiments were performed for $N_{ADC,k} = 4$, $N_{DAC,k} = 12$ and $N_{comp} = 20$. Fig. 6a shows that the greater analogue noises are, the greater decrease in the total performance of IP ADC is. The developed tools enable accurate assessment of this decrease.

In the fourth series of experiments (Fig. 6b), influence of the errors of the gains C_k setting was analysed. Errors were simulated according to the model: $C_k^{(err)} = (1+\delta_C)C_k$, where $C_k^{(err)}$ denotes the disturbed value of the gain, δ_C is the disturbance coefficient, and C_k is the nominal value defined using methods presented in [8-9], $L_k = C_k^{-1}$. The experiments were performed for $N_{ADC,k} = 4$, $N_{DAC,k} = 12$, $N_{comp} = 20$ and $\sigma_{an} = 25 \cdot 10^{-6}$ [V]. Fig. 6b shows that the acceptable level δ_C of C_k deviations, for which the performance of IP ADC remains unchanged, is not greater than ±0.2%.

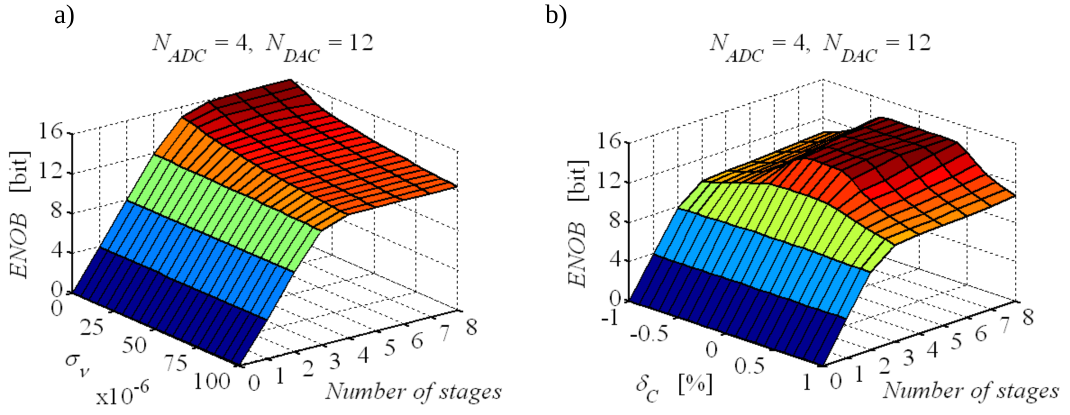

Figure 6. ENOB versus number of stages for different level σ_v of analogue noises (a), and different level δ_C of the gains C_k setting errors (b).

IV. Conclusions

The results of investigations show that the models, methods and simulation tools, proposed and presented in the paper, enable efficient analysis of IP ADC work and definition of the most appropriate parameters of main components of the converter which provide the required final performance of IP ADC. The developed analytical tools permit to analyse and compare IP ADC with different configurations of internal components and their parameters. These tools also enable to perform a simulation comparison of expected performance of IP ADC with performance of existing pipeline ADC. The results of the paper can be used at the initial stages of IP ADC design for effective choice of suitable architecture and parameters of the internal components of IP ADC as well as preliminary assessment of expected IP ADC performance achievable under assumed conditions.

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