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Nonidealities Study of a Continuous-Time Delta-Sigma Modulator Using VHDL-AMS Modelling

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Abstract- In this paper, a complete high-speed Continuous-Time Bandpass Delta-Sigma modulator for digital receiver applications is modeled, using VHDL-AMS. The main Continuous-Time Delta-Sigma modulator's nonidealities such as excess loop delay, clock jitter and multi-bit feedback DAC element mismatch in the modulator loop are also modeled and their effects evaluated. An accurate understanding of these non-ideal phenomena allows to estimate the limits of the modulator and hence to design more robust building-blocks.

I. Introduction

Conventional radio receiver front-end architectures are basically composed by an antenna, an analog signal processing stage, a mixed-signal stage (analog-to-digital converter - ADC) and a digital signal processor (DSP). Shifting the ADC closer to the antenna, allows to simplify the overall system design and to eliminate some analog functions such as amplifiers, filters and mixers (integrated circuits and/or external components). These functions can be easily implemented in the digital domain, reducing the receiver complexity and therefore the power consumption. Nevertheless, the bottlenecks are the ADC required specifications which become more severe with the antenna closeness.

Bandpass Delta-Sigma converter architectures incorporate the idea of digitizing the analog signal directly into intermediate frequency. This type of converter allows reducing analog hardware and further realization of fully-integrated software-programmable RF receivers (SDR – Software Defined Radio [1]). For this reason, several published single-bit Continuous-Time (CT) Delta-Sigma ($\Delta\Sigma$) modulators can digitize signals from 800MHz to 1GHz [2-4]. However, CT $\Delta\Sigma$ modulators suffer from performance degradation due to nonidealities such as excess loop delay, clock jitter and multi-bit feedback DAC element mismatch in the modulator feedback loop. However, due to their different mechanisms and different occurring points inside the modulator, their effects are different. To ensure a successful design, a careful understanding of these non-ideal phenomena is required. In this paper, the main $\Delta\Sigma$ modulator nonidealites are modeled. To evaluate the nonidealites effects, the resulting models are applied to a high-speed CT $\Delta\Sigma$ modulator.

II. VHDL-AMS Continuous-Time Delta-Sigma Modulator Behavioral Model

A CT $\Delta\Sigma$ modulator was modeled using VHDL-AMS. The architecture modeled is based on an association of resonators with two different types of feedback Digital-to-Analog Converter (DAC). This architecture allows the achievement of a higher order noise-shaping which maintains the modulator stability. The DAC used are return-to-zero (RZ) and half-return-to-zero (HRZ). The quantizer implements a 3-bit flash architecture. Figure 1 shows the Continuous-Time Delta-Sigma modulator architecture.

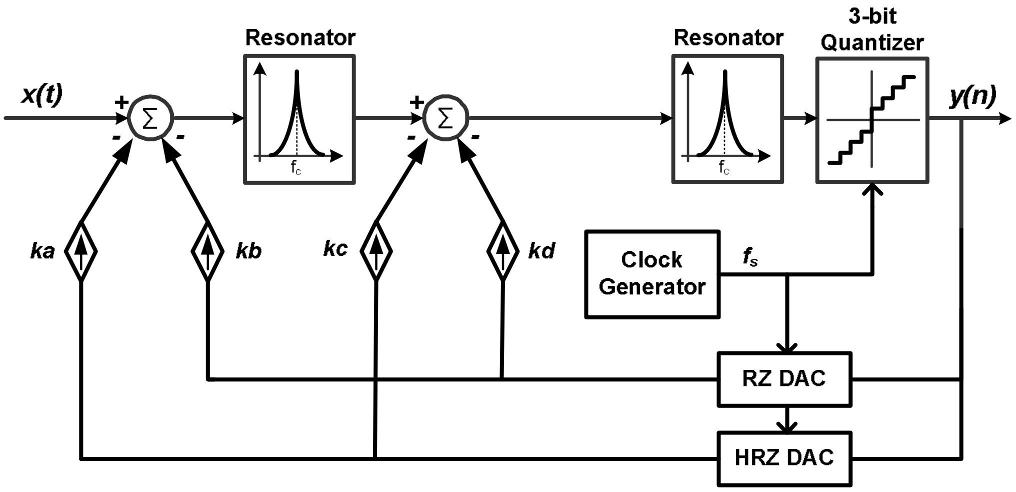

Figure 1. Continuous-Time Delta-Sigma Modulator Architecuture

This architecture, shown in Figure 1, was first simulated using just ideal blocks. This allows to validate the overall architecture and to estimate its ideal performance. After, nonidealities such as excess loop delay, clock jitter and multi-bit feedback DAC element mismatch was introduced. The aim is modelling a more realistic system and improves the robustness of the building-blocks.

II. Nonidealities Modelling

A. Excess Loop Delay

In theory, the quantizer and DAC currents react instantly to the clock edge, but in practice, the transistors in the quantizer and the DAC cannot commutate immediately. Hence, there is a delay between the clock edge and the response of the quantizer and the DAC: this delay is so called '*excess loop delay*'. Excess loop delay derives mainly from the quantizer delay and the finite switching time of DAC cells. If the excess loop delay is large enough to shift the falling edge of the DAC pulse beyond T_s (sampling period), thus it increases the order of the equivalent DT modulator by one [5]. Performance degradation and even instability may occur. To evaluate how the excess loop delay affects the noise-shaping performance, continuous-time domain simulation using ADVanceMS was performed. An "excess loop delay emulator" (Figure 2) was developed and applied to the quantizer and feedback DAC. Figure 3 presents output spectrum plots for the ideal case and the case with 20% period excess loop delay. It can be observed that the SNR loss increases when the excess loop delay increases. If the excess loop delay goes beyond 50% of T_s, the modulator goes unstable (the order of the equivalent discrete-time domain loop transfer function increases by one). To mitigate this effect, it is possible to adjust the feedback coefficients (ki's in Figure 1) to achieve the correct discrete-time domain transfer function for noise-shaping [6].

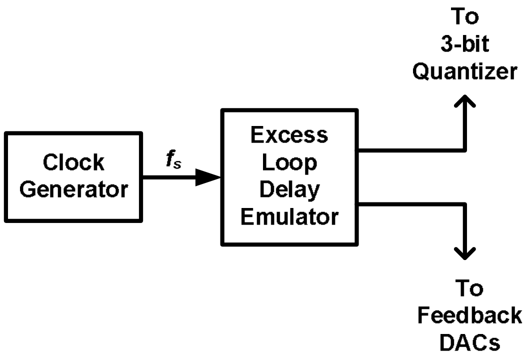

Figure 2. Excess Loop Delay Emulator

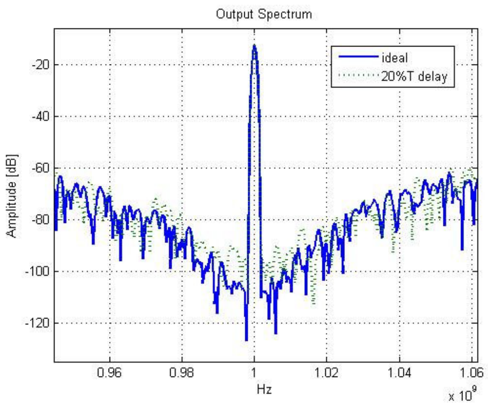

Figure 3. Effect of Excess Loop Delay

B. Clock Jitter

Jitter is defined as a random variation of a signal's significant instants from their ideal positions in time. In the case of clock jitter, the significant instants are the optimum sampling instants. CT modulators are more sensitive to clock jitter than DT modulators [5]. Both quantizer and feedback DAC are exposed to sampling error due to the clock jitter. The effects of clock jitter in the quantizer are noise shaped by the modulator so that it adds little noise to the system output. However, clock jitter in the feedback DACs generates noise which is not shaped and affects the modulator performance considerably. In order to evaluate this phenomenon, a "clock jitter generator" has been modeled using VHDL-AMS (Figure 4). It is based on a random number generator using the Gaussian distribution function. However, VHDL-AMS does not provide this type of distribution. We had therefore to create this function from the UNIFORM function (provided by VHDL-AMS). This function offers a pseudo random numbers sequence with a uniform distribution between] 0; 1]. The well-known transformation (1) to pass from a uniform distribution to a Gaussian distribution is Muller Box [7]:

$$v = m + std.\sqrt{(-2.\log(u_1))}.(\sin(2.\pi.u_2) \tag{1}$$

where:

v: Gaussian Distribution
(u1,u2): random functions
std: standard deviation
m: distribution average

Figure 5 shows the comparison of different variations of the clock jitter. Note that SNR degradation rises when the clock jitter increases.

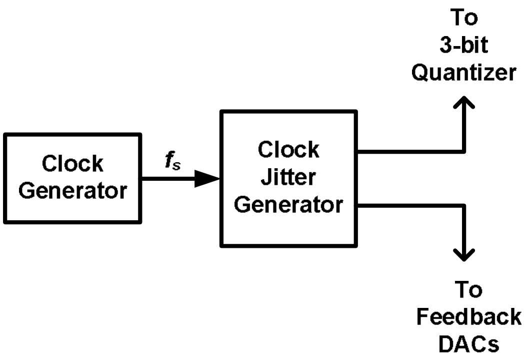

Figure 4. Clock Jitter Generator

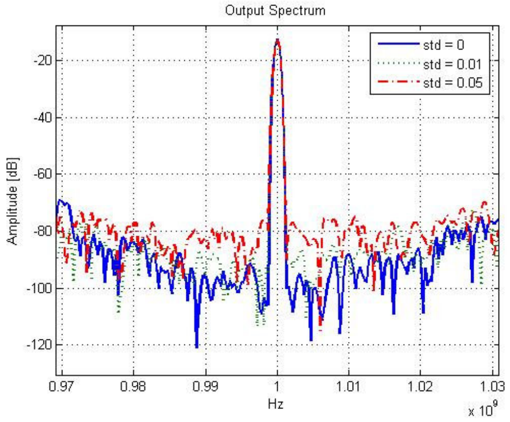

Figure 5. Effect of Clock Jitter

C. Multi-bit feedback DAC element mismatch

Usually, ΔΣ modulators employ are designed with a 1-bit quantizer (comparator) and consequently a 1-bit DAC in the feedback path. This category of DAC is inherently linear and do not introduce error in the main modulator path. Nowadays, there is an increasing interest to implement multi-bit ΔΣ modulators. It has several advantages compared to a 1-bit modulator, including the reduction of quantization noise and the improvement of SNR (6 dB per extra bit in the quantizer), the reduction of clock jitter sensibility and the system stability enhancement. However, multi-bit quantizer calls for multi-bit feedback DAC, which is affected by errors due to the mismatch between the DAC elements. The multi-bit feedback DAC element mismatch is very critical for the modulator performance. The nonlinearity coming from the feedback DACs is directly reinserted in the main modulator path, increasing the in-band noise-floor and reducing the SNR. To estimate how the mismatch between the DAC elements degrades the CT modulator performance, the feedback DACs were modeled taking into account the element DAC current variation (Figure 6). Figure 7 shows the output spectrum of linear and a nonlinear feedback DAC. It can be observed that the feedback DAC nonlinearity introduces strong intermodulation products in the signal band which elevate the noise-floor, and therefore the noise shaping performance is reduced significantly.

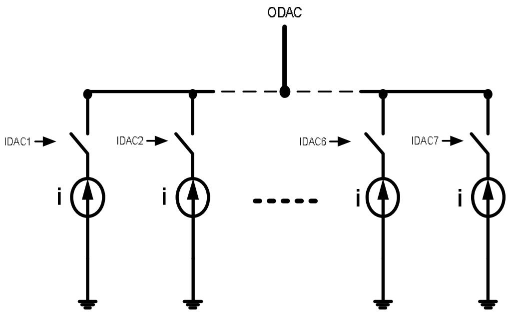

Figure 6. Feedback DAC structure

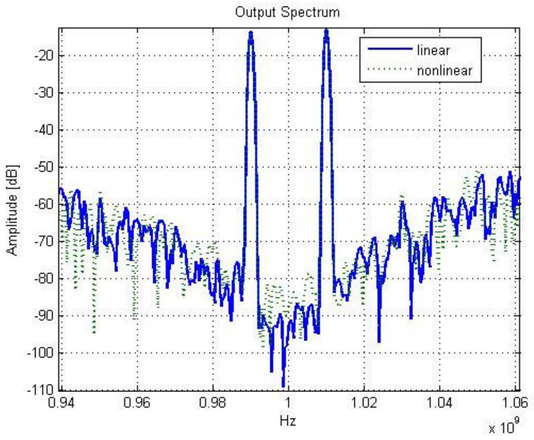

Figure 7. Effect of feedback DAC nonlinearity

V. Conclusion

A VHDL-AMS behavioral model of a high-speed Continuous-Time Delta-Sigma Modulator is presented in this paper. The main nonidealities of this type of modulator were also modeled and their effects evaluated. These nonidealites degrades the performance of the modulator, decreasing the SNR and introducing intermodulation products. The knowledge of the limitations of the modulator allows to take cautions in the design of the functional building-blocks, improving a more robust system.

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