

# Exponential Fit Test - Theoretical analysis and practically implementation

Josef Vedral

CTU Prague, Faculty of Electrical Engineering, Department of Measurement,  
Technicka 2, 166 27 Prague, Czech Republic  
e-mail: vedral@fel.cvut.cz

**Abstract** - ADC testing by means of exponential signal is presented in the article. Time and frequency analysis of the signal is performed and Signal-to-Noise Ratio and Effective Number of Bits is calculated by means of Best-Exponential Fit Test. The approach has been verified on 24-bit Flexible Resolution Digitizer PXI-5922 by National Instruments. Results comparable with classical sine-fit method indicate the possibility of consideration of the proposed method as an alternative digitizer test method.

## I. Introduction

The contemporary standard for digitizer dynamic parameters testing is set of methods deploying input pure sinuswave signal of a guaranteed quality [1]. The disadvantage of those methods is the necessity of low-distortion harmonic signal availability. Such a signal must be of significantly lower distortion than that of digitizer output, caused by its real features and quantizing noise. E.g. for 16-bit digitizer testing the sine wave of *THD* higher than 100 dB is required. Such a requirement can be fulfilled either by means of narrow-band frequency filtering or by means of frequency spectra complex subtraction of digitizer input and output signals [2]. The other option is polyharmonic signal deployment. One of the most natural polyharmonic signal is exponential signal that is easy to generate with high accuracy [3].

## II. Exponential Signal Generation

Exponential signal is generated out of rectangular signal by means of passive *RC*-element filtration, where time constant  $\tau = RC$ , see Figure1.

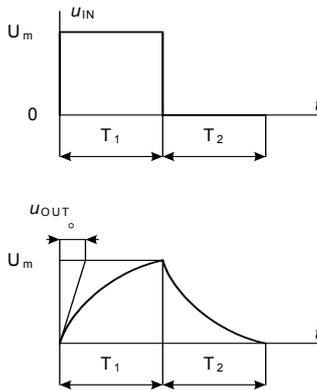


Figure1 Exponential signal generation

Output signal is defined as

$$u_c(t) = U_m \left( 1 - e^{-\frac{t}{\tau}} \right) \quad (1)$$

where  $U_m$  is input rectangular signal amplitude.

To achieve the final output steady-state signal difference from theoretical value less than the resolution of the tested digitizer with nominally  $n$  bits, the minimum ratio between  $T_1$  ( $T_2$ ) and time constant  $\tau$

$$T_{1(2)} \geq \tau(n+1) \ln 2 \quad (2)$$

For example, 16-bit digitizer requires the period of input rectangle  $T \geq 11 \tau$ .

For the duty factor  $T_1 = T_2 = T$  are the frequency spectra of both exponential curves identical:

$$A(\omega) = \frac{1}{\sqrt{1 + \left( \frac{\omega}{\tau} \right)^2}} \quad (3)$$

For  $\omega \gg \tau$  is  $A(\omega) = \tau/\omega$  and show linear amplitude decrease  $-20$  dB/dec., see Figure 2.

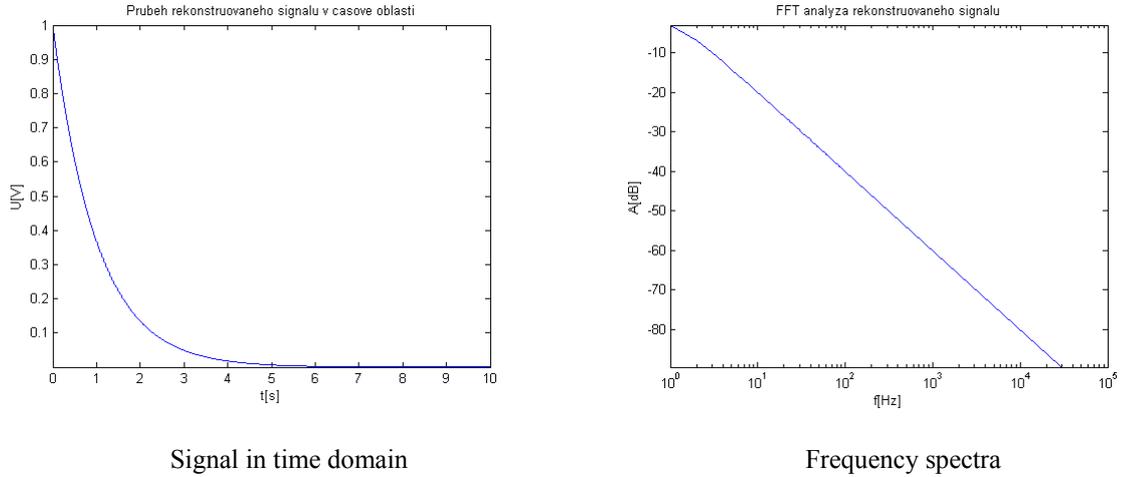


Figure 2 Exponential signal and its frequency spectra by  $\tau = 1$  s

### III. SNR and ENOB Calculation

According the definition, the ratio between *Signal to Noise Ratio* of ideal  $n$ -bit quantizer is [1]

$$SNR = 6,02n + 10,79 - 20 \log \frac{U_m}{U_{RMS}} \text{ (dB)} \quad (4)$$

where  $U_m$  is a maximum value and  $U_{RMS}$  is the *RMS* value of quantization error.

The third element of the equation shows the dependency of *SNR* on ratio between maximum and *RMS* input signal values (*Crest Factor*). As the *RMS* value of input exponential signal is

$$U_{RMS} = \sqrt{\frac{1}{T} \int_0^T \left( U_m \cdot e^{-\frac{t}{\tau}} \right)^2 dt} = \frac{U_m}{\sqrt{2}} \sqrt{\frac{\tau}{T} \left( 1 - e^{-\frac{2T}{\tau}} \right)} \quad (5)$$

And the crest factor

$$k_v = \frac{U_m}{U_{RMS}} = \frac{\sqrt{2}}{\sqrt{\frac{\tau}{T} \left( 1 - e^{-\frac{2T}{\tau}} \right)}} \quad (6)$$

The *SNR* of ideal  $n$ -bit quantizer is

$$SNR = 6,02n + 10,79 - 20 \log \frac{\sqrt{2}}{\sqrt{\frac{\tau}{T} \left( 1 - e^{-\frac{2T}{\tau}} \right)}} \text{ (dB)} \quad (7)$$

The Exponential Fit Test is based on best fitting of exponential signal to the tested digitizer output signal. If (equidistant in time) samples are acquired from one period of output signal, it is possible to reconstruct the exponential signal by means of least-square fitting method

$$x_n = Ae^{-Bt} + C \quad (8)$$

where  $A$  is the reconstructed signal amplitude,  $1/B$  is its time constant and  $C$  is its DC value.  $RMS$  error of this fit  $E$  denotes the tested digitizer *Effective Number of Bits*

$$ENOB = n - \log_2 \left( \frac{E}{RMS_q} \right) \quad (9)$$

where  $n$  is the nominal number of digitizer bits and  $RMS_q$  is the RMS value of its quantizing error.

#### IV. Testing high resolution system with Exponential Signal

This method has been implemented in 24-bit Flexible Resolution Digitizer NI PXI-5922 by National Instruments. External pulse square generator has been used to generate input rectangular signal in frequency range to 50 kHz. The time constant was chosen to  $\tau = 1$  s, where the amplitude spectrum is constant to frequency 100 kHz. For comparison purposes between standard and exponential test, the sampling frequency 60 kHz and 2 097 051 acquired samples has been chosen, see Figure 3.

Because the *Exponential Fit Test* is sensitive to precise identification of exponential start, the reconstructed signal has been divided into two parts according to its first derivative polarity before fitting, see Figure 4.

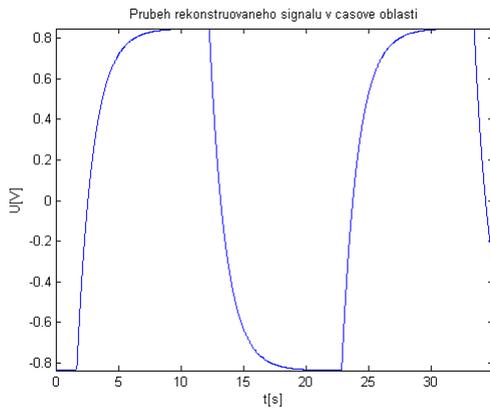


Figure 3 Test Signal in Time domain

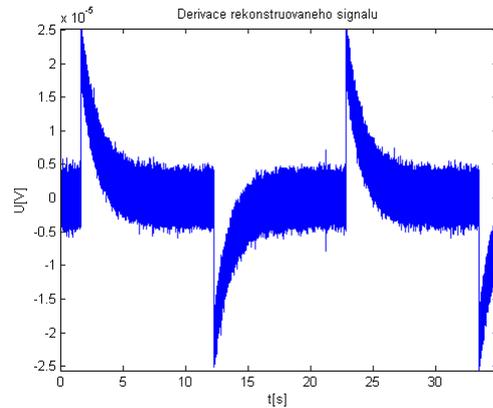


Figure 4 First Signal Derivative in Time Domain

By comparing fittings from both polarities, it is possible to identify differences in *SINAD* and *ENOB* for different input signal polarities, caused e.g. by digitizer characteristics hysteresis.

Resistor of 1 M $\Omega$  and capacitor of 1 $\mu$ F by ARCOTRONICS, with minimum dielectrical absorption MKT (10ppm) has been used for *RC*-element design. Low-noise operational amplifier OP177 with differential gain  $10^6$  has been used for impedance insulation. Its slew rate is 0,6 V/ $\mu$ s and thermal drift 1  $\mu$ V/K does not practically influence generated signal parameters. Parasitic inductance of the used capacitor has, on the contrary, significant influence.

#### V. Comparison results

For *Exponential Fit Test* verification in the 24-bit Flexible Resolution Digitizer NI PXI-5922 by National Instruments has been used. It was run at 200 kSa/s being fed by Sine Fit Test in the frequency range up 20 Hz to 100 kHz and amplitude 2  $V_{pp}$ . The achieved *SINAD* = 103 dB corresponds to *ENOB* = 16,8 bits.

Using exponential signal as the digitizer input, the *SINAD* = 106 dB corresponding to *ENOB* = 17,3 bits has been achieved. The difference of 1,5 bit was most probably caused by exponential signal frequency spectra decrease.

This method has been implemented in FPGA Start Development Kit Cyclone II by Altera. Internal controlled generator from FPGA has been used to generate input rectangular signal in frequency range from 20 Hz to 30 kHz. The time constant was chosen to  $\tau = 1$  s where the spectrum is linearly decreasing in this frequency range with decrease -20dB/dec. For comparison purposes between standard and exponential test, the sampling frequency 60 kHz and 2 097 051 acquired samples has been chosen.

Exponential Fit Test verification in the FPGA by Altera with nominal resolution 24 bits has been used. It was run at 60 kSa/s being fed by Sine Fit Test in the frequency range up to 20 Hz to 20 kHz. The achieved  $SINAD = 90,9$  dB corresponds to  $ENOB = 14,8$  bits, see Fig.5.

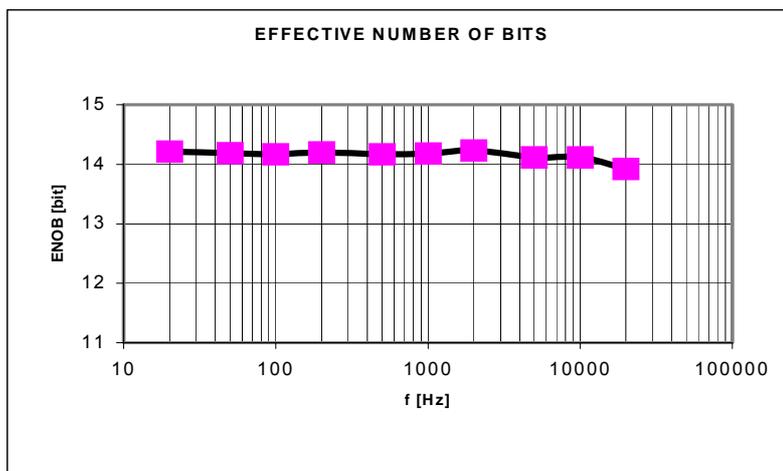


Fig.5  $ENOB$  plot for Sin Fit Test by FPGA Altera

Using exponential signal as the digitizer input, the  $SINAD = 86,6$  dB corresponding to  $ENOB = 14,1$  bits has been achieved. The difference of 0,7 bit was most probably caused by exponential signal frequency spectra decrease.

Achieved results prove the method applicability for dynamic testing of up to 16 bit digitizers, and method simplicity allows for embedded applications. The frequency spectra can be easily modified by changing the time constant of RC element.

## VI. Acknowledgement

This project is supported by the research program MSM6840770015 "Research of Methods and Systems for Measurement of Physical Quantities and Measured Data Processing" of the CTU in Prague sponsored by the Ministry of Education, Youth and Sports of the Czech Republic.

## References

- [1] IEEE Std. 1241-2000. IEEE Standard for Analog to Digital Converters. The Institute of Electrical and Electronics Engineers, Inc., New York, 2000
- [2] Slepíčka, D. - Dallet, D. - Shitikov, V. - Barbara, F.: Posteriori Frequency Spectrum Correction for Test Signal Imperfections in ADC Testing. In IMTC/2007 *IEEE Instrumentation and Measurement Technology Conference Proceedings* [CD-ROM]. Warsaw: IEEE, 2007, ISBN 1-4244-1080-0.
- [3] Holcer, R., Michaeli, L.: DNL ADC Testing by the exponential shaped voltage. In *IEEE Transaction on Instrumentation and Measurement*, ISSN 0018-9456, vol. 52, No. 3, (2003), p.946-949.
- [4] Michaeli, L., Sakmár, M., Šaliga, J.: Some Errors of Analogue Signal Sources for ADC Exponential Stimulus Histogram Test. In TC4 International Workshop on ADC Modelling and Testing, Technical University of Asachi, pp.51-56, ISBN 978-973-667-264 .
- [4] 24-bit Flexible Resolution Digitizer NI PXI-5922, <http://www.ni.com>
- [5] Cyclone II FPGA Starter Development Kit, <http://www.altera.com>.