State of Art on the Tests for ΣΔ ADC

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***Abstract*:** The paper deals with the state of art on the tests for both ΣΔ modulators and ΣΔ Analog to Digital Converters (ADCs). Particular aspects are highlighted concerning the tests for the innovative architectures based on the Band Pass ΣΔ ADC. The analysis of the tests is carried out in conjunction with the discussion about the applicability of the procedures included into the IEEE Standard 1241. Therefore, three fundamental groups of tests are defined: (i) tests according to the IEEE Standard 1241, (ii) tests included into the IEEE Standard 1241 but executed in a different way from the Standard, and (iii) tests pointed out to evaluate the specific characteristics of the ΣΔ modulator not included into the IEEE Standard 1241.

Keywords: Analog to Digital Converter, Testing, ΣΔ Modulator.

I. Introduction

The ΣΔ Analog to Digital Converters (ADCs) evidence particular characteristics that are attractive in many applications. Numerous and different architectures are proposed for implementation into the telecommunication systems [1]-[3].

The large diffusion in this very important and advanced technical applications justifies the interest for new questions regarding the tests and the metrological characterization of the ΣΔ ADCs. New questions arise from both the operating mode and the innovative architecture. In order to discuss in dept about these questions, the summarization of the ΣΔ ADC architectures behavioral characteristics is basic. For sake of completeness, in the following the characteristics of the ΣΔ ADC are analyzed by clustering the different architectures in groups marked by distinctive operating features. For sake of brevity, only the fundamental groups are shown. Nevertheless, more groups or sub-groups can be fixed on the basis of the characteristics pointed out.

The ΣΔ ADC architecture is constituted by two basic blocks: the ΣΔ modulator and the digital output filter. The ΣΔ modulator is a non-linear system including: (i) analogue input filter, (ii) quantizer block, and (iii) Digital to Analogue Converter (DAC) [4], [5]. The main characteristics and the connections among these blocks determine the different ΣΔ modulator architectures.

The ΣΔ modulator architecture can be distinguished in two groups: (i) Low Pass (LP) and (ii) Band Pass (BP) modulator [4], [5]. The BP ΣΔ modulator has a limited input bandwidth centered around a quarter of the sampling frequency (f_s) and the output is base-band translated by the Digital Down Converter (DDC). At the output the signal is low pass filtered and the two components In phase (I) and in Quadrature (Q) are available.

Other groups can be characterized on the basis of the number of quantizer levels. The quantizer block can works with one or several levels and it is the cause of the quantizer error shaped by the modulator's noise transfer function [4], [5]. The noise shaping is achieved by creating the feedback loop around the cascade of the analogue input filter and the quantizer block. The number of quantizer levels establishes the bit number of the DAC [6].

Further groups can be characterized on the basis of the number of quantizers. If only one quantizer is included in the architecture, the modulator is denoted as Single Quantizer Loop (SQL) [7]. The transfer function order of SQL depends on (i) the number of integrators, (ii) the feedback loops, and (iii) the connection among them. There are SQL architectures employing time delay blocks to modify the transfer function in order to overcome the stability problems [4], [5] that can occur with high order transfer function. In order to maintain the benefits of the high order SQL and to overcome the stability problems the Multistage Noise Shaper (MASH) ΣΔ architecture is introduced [8]. The MASH architecture consists of the cascade of a number of stages each one constituted by a SQL and feed by the quantizer error of the previous one.

The hardware of the ΣΔ modulator introduces the principal source of alteration from the ideal behavior of the ADC. In fact the other components, the DDC and the digital output filter, introduce negligible error [9].

The first aspect, following the previous considerations, is that both the definitions and the test procedures of the IEEE Standard 1241 [10] in part can be applied to the ΣΔ ADC, and in part must to be redefined.

Indeed, the test procedures included into the IEEE Standard 1241 are pointed out for ADC with transfer function not modifying the spectral frequency range of the input signal. As a consequence, this Standard can be utilized for testing the LP ΣΔ ADCs. For testing the BP ΣΔ ADCs the Standard can not be utilized in all the

recommendations. Indeed, the transfer characteristic of the modulator is BP, and the operations executed into the BP ΣΔ ADC don't permit the correlation between the characteristics of the input and the output signals in the time and in the frequency domain [11]. Differently, this correlation is permitted from the operations executed by the LP ΣΔ ADCs.

The second aspect is the possibility to adapt some test procedures of the IEEE Standard 1241 to the ΣΔ ADCs in order to obtain an easily generation, with high accuracy, of the stimulus signal. Examples are constituted by: (i) the Signal to Noise Ratio (SNR) test by using the digital bit stimulus in the place of the sinusoidal one [12], [13], and (ii) the nonlinearity test by using a pseudo-random binary stimulus [14], [15].

The third aspect is the demand to develop specific tests to evaluate the functional characteristics of some components. An example is constituted by the tests for the evaluation of (i) integrator leakage [16], [17], (ii) modulator performances [18], and (iii) the noise transfer function of the converter [19].

Therefore, the test and the characterization of the ΣΔ ADCs need (i) to overcome the problem to apply the IEEE Standard 1241, and (ii) to introduce new and specific test procedures. On the basis of these considerations, the interest is devoted to discuss about the state of art on the tests pointed out for the ΣΔ ADC architectures.

The paper is organized as follows: initially, the applicability of the IEEE Standard 1241 to test the ΣΔ ADC is discussed. Successively, specific tests are considered (i) in the frequency domain for both the SNR and the nonlinearity estimation by means of the impulsive modulated signals or by analogue signal injected in the feedback loop, (ii) in the time domain for the integrator leakage measurement, and (iii) in the time and the frequency domain for the modulator tests.

II. Applicability of the IEEE Standard 1241 to test BP ΣΔ ADCs

According to the IEEE Standard 1241, the ADC characterization should be done by evaluating the static and the dynamic characteristics. Moreover, the evaluation of the gain error, offset error, integral nonlinearity, and differential nonlinearity can be done by the histogram tests [4], [10], [20]-[22]. Other parameters can be estimated typically by the spectral analysis [23]-[25]. Some parameters usually estimated are: SNR, SIgnal to Noise And Distortion to ratio (SINAD), Effective Number Of Bits (ENOB), Total Harmonic Distortion (THD), and the Spurious Free Dynamic Range (SFDR).

The test procedures of the IEEE Standard 1241 were defined only for conventional ADC converting the input signal with the frequency spectrum included into the range [0, f_s/2]. The IEEE Standard 1241 can be used in the case of the LP ΣΔ ADC. The transfer function of this converter is similar to that of the other architectures of conventional converters, and both the static and dynamic tests can be able to characterize this converter [5]. In fact, the ADC makes the conversion of the input signal from the analog to the digital domain without to change the fundamental characteristics of the input signal in the time and in the frequency domain. The only effect is the introduction of the noise floor and harmonics as a consequence of the nonlinearity of the hardware devices.

The transfer characteristic of the BP ΣΔ ADC is different. In fact, the modulator output is centered at the quarter of the sampling frequency. Successively, it is base-band translated before the digital output filter of the converter. These operations are fundamentals because (i) increase the number of bits at the output, and (ii) decrease the data rate. The signal in base-band corresponds to the I/Q components of the input. Therefore, the BP ΣΔ ADC modifies the spectral trend of the input signal. The procedures for testing the conventional ADC are not able to be used in these architectures and the definitions of the Standard must to be redefined.

The static tests presented in [10] need the constant input signal in order to determine some parameters. In this case the output of the BP ΣΔ ADC is zero because the input is out of the band. Similar considerations can be done for the dynamic tests. As an example, the high harmonics produced by the nonlinearity of the hardware components can be out of the frequency band considered. Therefore, the parameters SINAD and THD have different significance if evaluated in the band or out of the band of the BP ΣΔ ADC. Moreover, the BP ΣΔ ADCs have a different behavior from the conventional ADCs, the output is not correlated with the input signal. Therefore, some parameters as SINAD, THD, ENOB, SNR, SFDR, nonlinearity must to be redefined.

III. Tests for ΣΔ ADCs

The previous analysis concerning the behavioral characteristics related to the architecture of the ΣΔ ADCs and the applicability of the IEEE Standard 1241 addresses towards a proposal to cluster the tests in three groups:

1. tests according to the IEEE Standard 1241,
2. tests included into the IEEE Standard 1241, but executed in a different way from the Standard. This group includes the evaluation of the SNR and the nonlinearity test,
3. tests not included into the IEEE Standard 1241 and pointed out to evaluate the working characteristics of the ΣΔ modulator. This group includes the tests for (i) the evaluation of the integrator leakage, and (ii) the assessment of the operations performed by the modulator and the ADC.
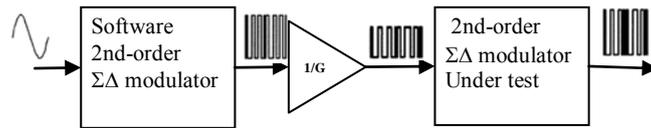
Fig.1   Block scheme for testing the 2nd order ΣΔ modulator
by means of digital bit stimulus.

A. Tests according to the IEEE Standard 1241

In the previous paragraph the applicability of the IEEE Standard 1241 for testing the ΣΔ ADCs is discussed. For the LP ΣΔ ADCs all tests of the IEEE Standard 1241 can be applied, in fact the transfer characteristic of this converter is similar to that of the conventional ADCs. For the BP ΣΔ ADCs some test procedures cannot be applied.

B. Tests included in the IEEE Standard 1241, but executed in a different way

In the following the tests are examined for the SNR estimation and the nonlinearity evaluation. The innovations consist of the introduction of the new digital test stimulus that guaranties high accuracy and low cost generation.

SNR test
In literature [12], [13] the innovative method for the SNR estimation in the case of ΣΔ ADC utilizes different test stimuli that can be easily generated with high accuracy. In particular, the innovative test procedure is proposed for the second order SQL LP ΣΔ ADC.
The test method uses a sinusoidal waveform coded by the ideal model of the ΣΔ modulator. The block scheme of the procedure is shown in Fig.1. The modulator under test is feed by the coded sine wave by means of the amplifier with gain 1/G, where G is the gain of the modulator. In the actual modulator the output differs from the input and the FFT is used to estimate the SNR after the output filter.
The results of the experimental tests show as in particular condition the maximum error in the SNR estimation respect the SNR estimated with a sinusoidal input signal is down to 3dB.

Nonlinearity test
The nonlinearity phenomenon, taken into account by the IEEE Standard 1241, provokes at the output of the ADC a lot of inconveniences, as: noise floor, noise modulation, and distortion.
In order to guaranty the signal with high accuracy, in [26] the use of the Maximum Length Sequence (MLS) is proposed. This test signal is used to measure the distortion at the output of the fourth-order ΣΔ LP ADC. The MLS is a pseudo-random binary signal obtained from shift register connected with exclusive-or feedback structures [14]. The signal is generated with a period equal to $L=2^m-1$, where m is the shift register length. The measure of the nonlinearity is obtained by evaluating the cross correlation between the input and the output of the ΣΔ ADC [14], [15].
The MLS signal have the following advantages: (i) it is a two level signal, with an imposed amplitude, (ii) it is more simple to be generated, and (iii) it stimulates the nonlinearity at the specific dc input voltage level equal to the test signal imposed amplitude.

C. Test not included in the IEEE Standard 1241

In the following the tests are examined for the integrator leakage measurement, the in band noise evaluation and modulator characterization in both time and frequency domain.
The integrator leakage is a phenomenon present into a real integrator. The integrator leakage decreases the integrator accuracy and belongs to the source noise of the ΣΔ modulator. This effect is similar to a non unitary feedback into the integrator. The tests want to determine the value of this feedback. There are no tests for this parameters in the IEEE Standard 1241 because it is a particular parameter of the ΣΔ ADC architecture.
In [16] a technique for the integrator leakage test operating on first and second order LP SQL ΣΔ modulator is proposed. The stimulus is a digital sequence and the leakage estimation is obtained by the counter connected to the modulator output. Fig.2 shows the block scheme of the test. The output of the modulator is a signal carrying information on the difference between the mean value of the input signal and the output bit stream. The deviation of the output bit stream average value from the mean value of the test signal is due to the modulator integrator leakage.
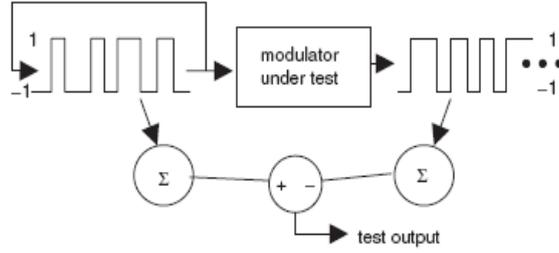
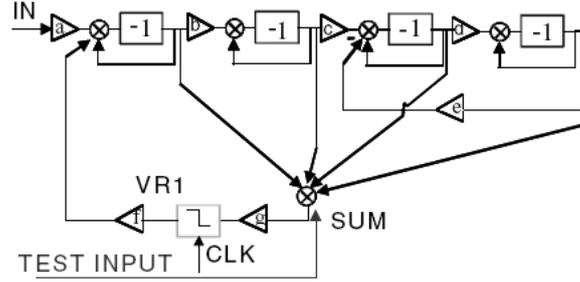Fig.2. Block scheme for testing the digital integrator leakage.

Fig.3. In-band noise evaluation test for modified 4th order $\Sigma\Delta$ ADC.

For the first order modulator a bit stream sequence with a nonzero mean value is used as the input signal [16], [17]. For the second order modulators there are two integrators with the respective leakages. The estimation of the first integrator leakage is determined by a counter fed by the output of the modulator. By taking into account the sum of the N output samples, where N is the multiple of the input sequence period, the counter output is, under the condition that the leakage of the integrators is small:

$$Counter \approx 2NQ\Delta p_1 \qquad (1)$$

where Q is the mean value of the input sequence, and Δp_1 is the first integrator leakage. In the case of input-referred to the offset of the modulator, the counter output is:

$$Counter \approx -N_{off} + 2NQ\Delta p_1 \qquad (2)$$

where N_{off} is the counter associated to the offset.
By using this Counter in conjunction with nCounter, obtained by feeding the modulator with the opposite input signal, the leakage of the first integrator and the offset of the modulator can be determined as:

$$\Delta p_1 \approx \frac{Counter - nCounter}{4NQ} \qquad (3)$$

$$off \approx \frac{Counter + nCounter}{-2N} \qquad (4)$$

For the estimation of the second integrator leakage a possible solution is to furnish directly at the second integrator the input sequence used for the first one. The same test principle can be used with a multi bit modulator.
For the in-band noise evaluation in [19] is proposed a method that uses the analogue sinusoidal test signal injected into the feedback loop with zero input, Fig.3. The spectral analysis of the output contains only the in-band noise plus the attenuated spectrum of the injected test signal. The sinusoidal test signal is characterised by frequency near to the cut-off frequency of the low-pass filter of the $\Sigma\Delta$ ADC.
In [18] is proposed a method to automatically model the behavioural characteristics of some architectures of $\Sigma\Delta$ modulators. The output signals of the considered modulator architectures are characterized by quite different trend in the time and in the frequency domain according to their different behavior. These different trends can be advantageous utilized to infer from the output signal the fundamental and useful parameters characterizing the architecture of the $\Sigma\Delta$ modulators under test. By clustering these parameters in homogenous classes the behavioral classification of the different architectures of the $\Sigma\Delta$ modulators can be carried out. The method is

organized with a hierarchical structure: the result of every test selects and configures the parameters of the successive test. Moreover, it requires that the ΣΔ modulator is fed by sine wave at a quarter of f_s, and the output signal is acquired and analyzed in both the time and the frequency domain.

In the frequency domain the classification method operates to distinguish between LP and BP ΣΔ modulator, and to identify both the SQL and the MASH architectures. In particular, the distinguish between LP and BP ΣΔ modulator is based on the analysis of the output signal of the modulator feed by the input sine wave. The position of the minimum of the spectrum permit the classification between LP and BP modulator. The identification among the SQL and the MASH architectures is performed on the basis of the slope of the decreasing zone characterizing the noise shaping of the normalized PSD. In fact, can be defined the parameter ζ as:

$$\zeta = \frac{f_k}{f_w} \tag{5}$$

where f_k, is the frequency corresponding to the reduction of 5% of the maximum value of the fitting curve of the noise shape in the normalized PSD, as is shown in Fig.4, and f_w is equal to the input sine wave frequency for the LP modulator and it is equal to $f_s/4$ for the BP modulator. The MASH architecture is identified by $\zeta > 0.65$.

Other tests are pointed out into the time domain to evaluate the levels of the quantizer block inside the SQL architecture, and to detect the number of cascaded stages inside the MASH architecture. To obtain these parameters the histogram of the modulator output is build. The number of levels detected in this histogram permit to evaluate the bit number of the quantizer for SQL architecture and the number of stages inside the MASH architecture.
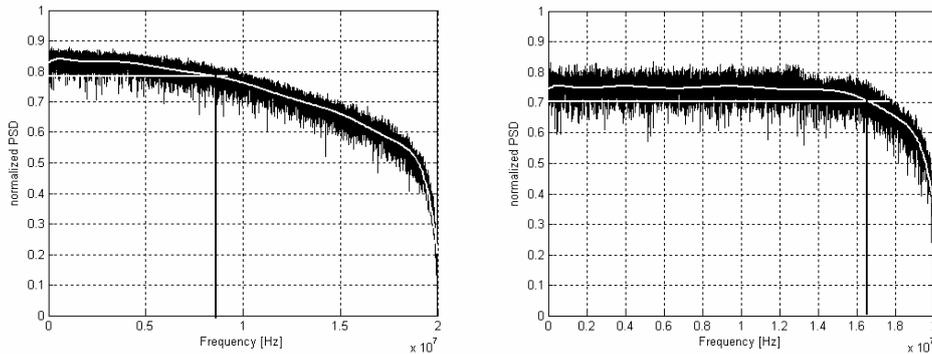

Fig.4   Evaluation of f_k for MASH (left) and SQL (right) BP architecture.

V. Conclusions

According to the new questions arising from the architectures of both Low Pass (LP) and Band Pass (BP) ΣΔ ADCs, the state of art on the tests is summarized.

It is highlighted the limited use of the IEEE Standard 1241 in the case of the BP ΣΔ ADCs, according to their innovative architecture.

The analysis of the tests is carried out in conjunction with the discussion about the applicability of the procedures included into the IEEE Standard 1241.

Three fundamental groups of tests are defined for the ΣΔ ADCs: (i) tests according to the IEEE Standard 1241, (ii) tests included into the IEEE Standard 1241 but executed in a different way from the Standard, and (iii) tests pointed out to evaluate the specific characteristics of the ΣΔ modulator.

References

[1]   M.I. Mathew, C.P. Lewis, "Design of sigma-delta modulation converters for telecommunication applications" IEE Col. on Adv. A/D and D/A Conv. Tech. and Appl., 8 May 1989, pp. 6/1 - 6/8.
[2]   F. Henkel, U. Langmann, "A sixth-order continuous-time quadrature bandpass sigma-delta modulator for UMTS low-IF receivers and a study of the inherent excess loop delay effect", Proceedings IEEE Intern. SOC Conference, 17-20 Sept. 2003, pp. 267 – 268.
[3]   R. del Rio, J.M. de la Rosa, F. Medeiro, B. Perez-Verdu, A. Rodriguez-Vazquez, "High-performance sigma-delta ADC for ADSL applications in 0.35 μm CMOS digital technology", The 8th IEEE

International Conference on Electronics, Circuits and Systems, ICECS Volume 1, 2-5 Sept. 2001, pp. 501 - 504 vol.1.

[4]   P.G.A. Jespers, "Integrated Converters D to A and A to D Architectures, Analysis and Simulation", Oxford Univ. press, 2000.

[5]   S.R. Norsworthy, R. Schereier, G. C. Temes, "Delta-Sigma Data Converters: theory, design, and simulation ", IEEE press 1997.

[6]   A. Tabatabaei, B.A. Wooley, "A wideband bandpass Sigma-Delta modulator for wireless applications", Digest of Technical Papers of IEEE Symposium on VLSI Circuits,. 17-19 June 1999, pp.91–92.

[7]   Th. Georgantas, St. Bouras, "Report on low power design techniques for data converters", INTRACOM Editor, ICCS-NTUA, Dec. 1998.

[8]   B.R. Rusu, B.R. Jose1, M. Ismail1, H. Tenhunen1, "A dual-band Sigma-Delta modulator for GSM/WCDMA receivers", Proc. of International XIX Conf. on Design of Circuits and Integrated Sys. DCIS 2004, Bordeaux, France, November 2004, pp. 673-676.

[9]   P. Arpaia, F. Cennamo, P. Daponte, H. Schumny, "Modeling and characterization of Sigma-Delta analog-to-digital converters" IEEE Trans. on Instrum. and Measur., Vol. 52, No. 3, June 2003.

[10]   IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters - IEEE 1241-2000.

[11]   M. Kollar, L. Michaeli, J. Saliga, "Parameters of band pass $\Sigma\Delta$ ADC and comparison with the standard ones", 14th IMEKO Symp. on new Techn. and Instrum., Jurata Poland 12-15 sept. 2005, pp. 617-621.

[12]   C.K. Ong, K. Cheng, Li-C. Wang, "A New Sigma–Delta modulator architecture for testing using digital stimulus", IEEE Trans. on Circ. and Sys. I, Vol. 51, Issue 1, Jan 2004, pp. 206 - 213.

[13]   M.F. Toner, G.W. Roberts, "A BIST scheme for an SNR test of a sigma-delta ADC" Proceedings on International Test Conference, 17-21 Oct. 1993, pp. 805 - 814.

[14]   D.D. Rife, L. Vanderkooy, "Transfer-function measurements with maximum-length sequences," J. Audio Eng. Soc., vol. 37, 1989 June, pp. 419-444.

[15]   C. Dunn, M.0. Hawksford, "Distortion immunity of MLS-derived impulse response measurements", J. Audio Eng. Soc., vol. 41, 1993 May, pp. 314-335.

[16]   G. Leger, A. Rueda, "Digital test for the extraction of integrator leakage in first- and second-order Sigma Delta modulators", IEE Proceedings on Circuits, Devices and Systems Vol.151, Is. 4, 12 Aug. 2004, pp. 349 – 358.

[17]   G. Leger, A. Rueda, "Simple BIST for integrator leak in second order double-loop sigma-delta modulators". Proc. Int. Mixed-Signal Test Workshop, Seville, Spain, June 2003, pp. 53–57.

[18]   D.L. Carnì, D. Grimaldi, L. Serratore, "Time and frequency domain tests for $\Sigma\Delta$ modulators", 14th IMEKO TC-4 Inter. Symp., Gdynia/Jurata, Poland, 12-15 September, 2005, pp.627-631.

[19]   D. De Venuto, "New Test for High Resolution $\Sigma\Delta$ ADC's by using the Noise Transfer Function Evaluation", Proceedings. 5th Intern. Symp. on Quality Electr. Design, 22-24 March 2004, pp. 81 – 85.

[20]   F. Azais, S. Bernard, Y. Bertrand, M. Renovell, "Implementation of a linear histogram BIST for ADCs" Proc. of Design, Automation and Test in Europe. Conf. and Exhib., 13-16 March 2001, pp. 590 - 595.

[21]   M. Renovell, F. Azais, S. Bernard, Y. Bertrand, "Hardware resource minimization for histogram-based ADC BIST", Proceedings of 18th IEEE VLSI Test Symposium, 30 April-4 May 2000, pp. 247 - 252.

[22]   F.A.C. Alegria, A.M. da Cruz Serra, "Overdrive in the ramp histogram test of ADCs", IEEE Trans. on Instrumentation and Measurement, Volume 54, Issue 6, Dec. 2005, pp.2305 – 2309.

[23]   M. Burns and G. W. Roberts, An Introduction to Mixed-Signal IC Test Measurement, 1st ed. Oxford, U.K. Oxford Univ. Press, 2001.

[24]   D. Bellan, A. Brandolini, and A. Gandelli, "ADC nonlinearities and harmonic distortion in FFT test," in Proc. IEEE Instrumentation Measurement Technology Conf., 1998, pp. 1233–1238.

[25]   N. Csizmadia and A. J. E. M. Janssen, "Estimating the integral nonlinearity of AD-converters via frequency domain," in Proc. Int. Test Conf., 1999, pp. 757–762.

[26]   C. Dunn, M.B. Sandler, "Measurement of nonlinearity in high-resolution sigma-delta converters", Second Intern. Conf. on Adv. A-D and D-A Conversion Techn. and their Applications, 1994, 6-8 Jul 1994, pp. 175 – 180.