

Methodology for Minimizing Timing Mismatch in Time-Interleaved ADCs

Michael Soudan¹, Francesco Zanini², Ronan Farrell³

¹ CTVR (NUIM, Ireland, +353 1708 6423, +35317086027, msoudan@eeng.nuim.ie)

² CTVR (NUIM, Ireland, +353 1708 6423, +35317086027, fzanini@eeng.nuim.ie)

³ CTVR (NUIM, Ireland, +353 1708 6197, +35317086027, rfarrell@eeng.nuim.ie)

Abstract - This paper describes a technique mitigating the impact of timing mismatches in time-interleaved analog-to-digital converters (ADCs). The systems signal-to-noise and distortion ratio (SINAD) and spurious-free dynamic range (SFDR) are increased by controlling the selection order of the channels ADCs in combination with oversampling and consecutive filtering. The proposed method requires only knowledge of the relative level of timing mismatch between the channel ADCs though not the precise magnitude of the mismatch. The impact of timing mismatch on the SINAD and advanced selection ordering schemes are discussed. Moreover, simulation results are presented comparing the figures of merit of existing techniques.

I. Introduction

Time-interleaved architectures are an effective way to implement high-speed analog-to-digital converters. Such an architecture combines multiple individual ADCs, called channels, into a single effective ADC by interleaving the input sampling times of the channel ADCs [1]. The resulting digital outputs are recombined digitally to produce an effective high sampling rate. This approach allows the use of channel ADCs that are many times slower than the overall system sampling rate. This facilitates the use of higher resolution ADCs or ADCs that have superior power efficiency.

However, mismatches between the individual channel ADCs, such as offset, gain, and timing, degrade performance and prevent us from achieving the full capability of the time-interleaved ADCs (TIADC). Timing mismatch, which arises due to clock skew and aperture uncertainty, is the most significant of the mismatch mechanisms as it remains the most difficult to correct. Successful techniques exist for correcting gain and offset mismatch [2,3], however techniques for correcting timing mismatch are either computational intensive or require some mechanism for determining, a-priori, the individual channel timing mismatch.

One successful technique for minimising timing mismatch in time-interleaved ADCs is by controlling the order in which channel ADCs are selected. By changing the order from a strict linear rotation, more complex selection patterns can be created which yield improved spectral results. The simplest of these techniques, randomisation, is effective in removing spurious tonal components at the expense of an increased noise floor [4,5]. A basic noise-shaping algorithm was presented by Vogel that utilises oversampling and groups of channel ADCs to shift the mismatch energy out of the band of interest [6], however, this was limited to just two groups. In this paper we propose a novel methodology for constructing an arbitrary number of groups and a simple selection algorithm that requires only the knowledge of the relative level of timing mismatch between the channel ADCs. It will be shown that this new approach provides significant performance improvements over existing techniques.

II. Impact of Mismatches

Channel mismatch is a static, or slowly changing, difference in either the time of the sample acquisition, the gain or offset of the ADC. Where as either signal noise or timing jitter can be assumed to be Gaussian and distributed equally across the bandwidth, channel mismatches result in tonal distortion throughout the spectrum. Timing mismatch is currently the most significant error mechanism in practical devices due to decreasing geometries and increased speeds. A TIADC with a normally distributed timing mismatch of 1% (standard deviation) will be limited to a maximum resolution of 7 bits without correction, irrespective of the resolution of the individual channel ADCs (Figure 1). This can be illustrated by considering that a 1% timing mismatch on a full-scale Nyquist-frequency signal can result in up to a 3.5% signal inaccuracy. The difficulty in achieving tight timing

synchronicity between channel ADCs has resulted in time-interleaved ADCs being focussed on power-efficient high-speed, low-resolution converters, such as recently demonstrated by Draxelmayr with a 6 bit, 600 MHz converter [7].

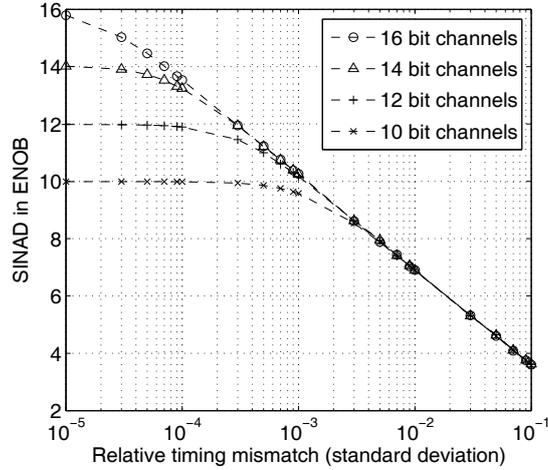


Figure 1 shows the impact of timing mismatch error on TIADCs with different channel resolutions.

The gain, offset and timing mismatch will result in undesirable tonal components. The location and magnitude of these spurious components has been derived by Vogel through a linear mismatch model for a time interleaved ADCs [8]. For a sinusoidal input of frequency ω_s , the spurs will occur at harmonics of the difference in the signal frequency and the channel ADC sampling frequency ω_c , and replicated at integer multiples of the channel ADC sampling frequency. Equation (1) shows the location of these spurs.

$$k(\omega_c \mp \omega_s) + m\omega_c \quad (1)$$

where k and m are integer numbers, representing multiple harmonics of the spurious tones. The distribution of these spurious components is illustrated in Figure 2 for the case of 16 channel ADCs.

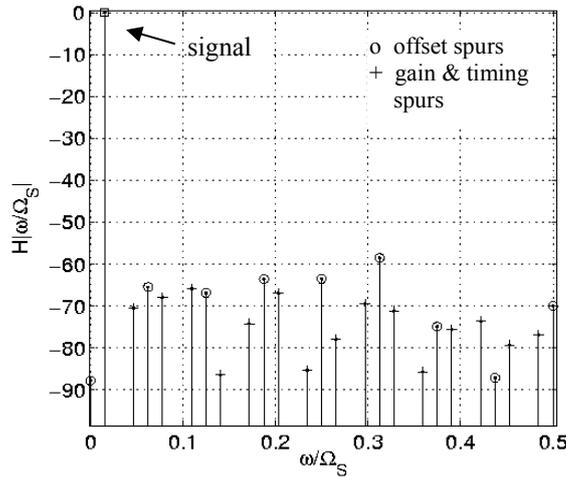


Figure 2. Magnitude spectrum of 16 ADCs with a constant selection sequence where Ω_s = effective system sampling frequency.

Randomization is one useful method for distributing the mismatch power over the frequency band and increasing the SFDR [4,5]. In this case, the order in which the channel ADCs sample the input signal is randomized. To achieve this in practice requires the use of one, or more, additional channel ADCs. The greater the number of these redundant channel ADCs R , the better the randomization effect. This is diagrammatically shown in Figure 3. However, it does not improve the overall SINAD, since the mismatch error power is only distributed and not reduced. To improve the SINAD we can oversample

the randomly sampled input signal and filter out all but the frequency band of interest. With ideal filters and assuming white noise, we can gain 3dB for every doubling of the oversampling ratio.

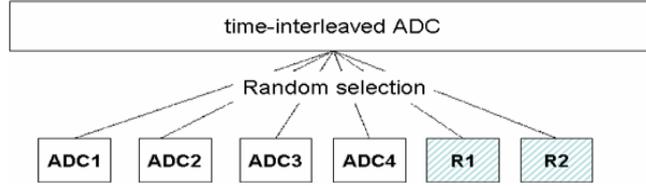


Figure 3: Randomised selection scheme utilising two additional channel ADCs.

Structured selection ordering techniques are able to improve the performance of mismatch affected TIADCs when significant oversampling is utilised. Vogel demonstrated a selection ordering scheme where the number of channel ADCs was doubled and sorted into two groups based on relative magnitude of timing mismatch. Each group was then alternately selected. Within each group, randomisation techniques were employed, ensuring good SFDR performance [4]. This architecture is shown for 4 ADCs per group in Figure 4. This scheme requires some knowledge of the relative level of timing mismatch between the channel ADCs though not the precise magnitude of the mismatch. This technique demonstrated a 6 dB performance improvement on in-band SINAD performance when utilising the same number of channel ADCs as randomisation.

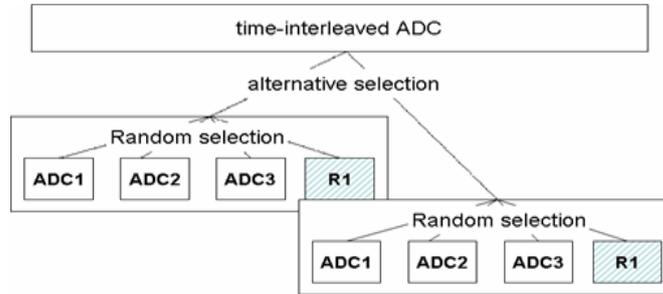


Figure 4: Randomised selection scheme utilising two additional channel ADCs.

Recent work from Vogel and Draxelmayr has concentrated on non-grouping algorithms for maximising the energy in the out-of-band spurs. These techniques show significant improvement in terms of overall SINAD performance but do not provide any guarantee on SFDR performance [7].

III. Methodology

The proposed method extends the technique presented in [6] to an arbitrary number of groups, which allows us to more aggressively concentrate mismatch energy in the out-of-band spurious frequencies while still employing randomisation techniques to guarantee SFDR performance (see Figure 5). By building more than two alternately selected groups, more mismatch energy can be concentrated in the spurious tones and therefore less energy is spread by randomization across the signal band.

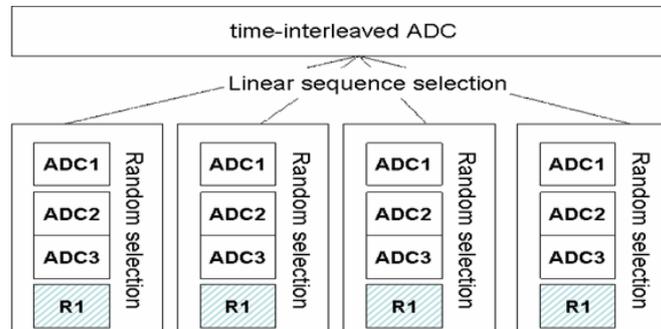


Figure 5. Selection scheme employing 4 alternately selected groups and a random selection sequence within each group.

The energy content of the spurious components from Equation (2) is given by the following expression [8]

$$Y(j\Omega) = \frac{2\pi}{MT} \sum_{k=-\infty}^{\infty} \begin{pmatrix} +\alpha[k]\delta(\omega - \omega_s - k\omega_c) \\ -\alpha[k]\delta(\omega + \omega_s - k\omega_c) \\ +\beta[k]\delta(\omega - k\omega_c) \end{pmatrix} \quad (2)$$

where the α and β terms represent the coefficients of the frequency components.

Optimising the ordering of the α and β terms such that the maximum energy is away from the signal band is numerically complex. However it can be shown that if the individual channel ADCs are sorted by their respective mismatch magnitude and assigned to groups based on that ordering (the least mismatch in group 1, etc), then a strict rotation selection routine results in a highly effective noise shaping profile [9]. The effectiveness of this approach is shown in Figure 6 where we have utilised 4 groups and our band of interest is $1/8 \Omega_s$. It can be seen that the tonal distortion has been removed and replaced with a white-like noise and tonal elements at quarter the effective system sampling frequency. The wave-like noise-distribution is a result of the limited number of randomisation ADCs available in a group, and it has been shown that additional ADCs will result in a flatter response [10].

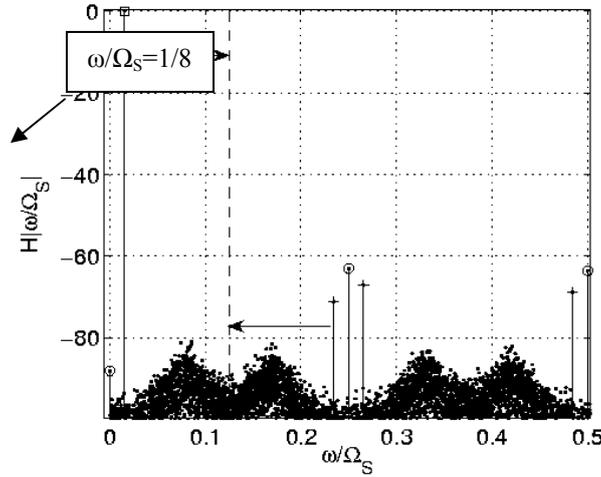


Figure 6. Spectrum of a TIADC with 16 bit channel ADCs, alternately selected groups and a randomisation scheme within each group (gain, offset and relative timing mismatch error of 0.1%, 0.1%, 1% respectively (standard dev.))

When using multiple groups, the effective channel ADC sampling frequency is determined by the number of time-interleaved elements within a group, thus

$$\omega_G = n\omega_c \quad (3)$$

where n is the number of ADCs per group, not counting the ADCs used for randomization.

Equation (1) indicates that the lowest spurious tone is therefore located at $\omega_G - \omega_s$ and that to prevent distortion, a filter should be applied at half the effective group sampling frequency and that the input signal must be restricted to:

$$\omega_{\max_signal} < \frac{1}{2}\omega_G = \frac{n}{2}\omega_c \quad (4)$$

The use of additional groups corresponds to increased oversampling. As the mismatch noise has been concentrated into the higher frequencies we can achieve improved robustness to mismatch at the expense of this additional sampling. The effective sampling rate of this time-interleaved ADC is dependent on the number of ADCs within a group (not counting those used for randomization). It has been shown by Jenq that the noise level, after randomization, is proportional to the standard deviation in the mismatch distribution within a group and with a small dependency on the numbers of ADCs within a group [11].

IV. Simulation Results

All presented simulation results have been calculated using channel ADCs with 16 bit resolution. For each of the 500 simulated outcomes, 4096 coherently sampled points were taken. To avoid the need to consider the in-band effect of real filters, an ideal brick-wall low-pass filter was used. For each group using randomization one additional ADC has been dedicated to that purpose. The individual channel mismatches were selected using a Gaussian distribution with a standard deviation of 0.1% (full-scale) for gain and offset, and 1% for timing mismatch error. The presented figures of merit are the average of all 500 outcomes.

In Figure 7a) and 7b) we compare the SINAD in effective number of bits (ENOB) respectively the SFDR in dB of TIADCs employing different selection schemes. To add comparison we have assumed that each system has an equal number of ADCs and an equal signal bandwidth. Where other techniques have an excessive bandwidth, we have assumed that an additional 3dB per octave performance can be achieved through filtering. Five techniques were considered, randomisation with no grouping, Vogel's optimised sequence selection, and three timing-mismatch ordering and grouping schemes (TMOG), with 2, 3, and 4 groups. The 2-group ordering and group scheme is that presented originally by Vogel [6].

As can be seen, the randomisation technique (when combined with the 3dB improvement through oversampling) will provide an SINAD performance of just below 8 bits. Using multiple groups demonstrates improved performance over randomisation and filtering, with an additional $\frac{3}{4}$ bits for using two groups, and an additional $1\frac{1}{2}$ bits when we use 4 groups. As can be seen in all of the randomisation techniques, there is the predicted small reduction in performance as the groups widen. If we examine the SFDR results in Figure 8 we see that using groups also significantly enhances performance with an additional 10 dB of improvement.

Vogel's latest work in optimised selection sequences shows superior performance in the area of SINAD when combined with the 3dB/octave improvement when scaling back to the same signal bandwidth as the 4-group system. However this technique is optimised for SINAD at the expense of SFDR and Figure 8 shows a significantly poorer performance [12].

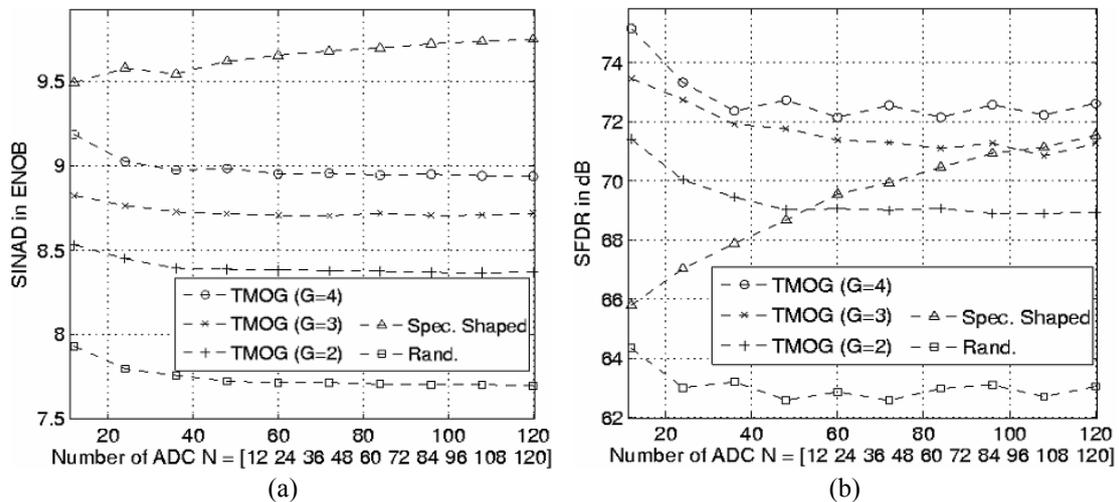


Figure 7. a) SINAD in effective number of bits and b) SFDR in dB for different selection techniques over the number of ADCs N

V. Conclusion

A selection ordering technique has been demonstrated which allows to improve the figures of merit by maximizing a number of spurious frequencies in the out-of-band region of the spectrum. By utilising additional ADCs, the figures of merit can be arbitrarily increased allowing for higher performance time-interleaved systems. Simulation results show that the proposed method compares favourably with existing selection ordering techniques when comparing both SINAD and SFDR. While this technique utilizes many additional ADCs, as silicon geometries shrink; using additional slower ADCs will become increasingly viable where benefits in cost and power efficiency can be achieved.

VI. References

- [1] W. Black, and D. Hodges, "Time interleaved converter arrays," *IEEE J. Solid-State Circuits*, vol. SC-15, pp. 1022-1029, Dec. 1980.
- [2] Jan-Erik Eklund, Fredrik Gustafsson, "Digital Offset Compensation of Time-Interleaved ADC using Random Chopper Sampling", *IEEE International Symposium on Circuits and Systems, ISCAS 2000*, vol.3, pp. 447-450, 2000.
- [3] Vincenzo Ferragina et al., "Gain and Offset Mismatch Calibration in Time-Interleaved Multipath A/D Sigma-Delta Modulators", *IEEE Transactions on Circuits and Systems*, vol. 51, pp. 2365-2373, 2004.
- [4] H. Jin, E.K.F. Lee, and M. Hassoun. "Time-interleaved A/D Converter with Channel Randomization", *IEEE Transactions on Instrumentation and Measurement*, vol. 54, Issue 1, pp. 425-428, 1997.
- [5] N. Duignan, R. Farrell, "An architecture for a reconfigurable charge-summation based ADC", *IEEE Conference on Advanced A/D and D/A Conversion Techniques and their Applications*, 2005
- [6] C. Vogel, V. Pammer, and G. Kubin, "A novel channel randomization method for time-interleaved ADCs", *Proceedings of the IEEE Instrumentation and Measurement Technology Conference*, vol. 1, pp. 150-155, 2005.
- [7] D. Draxelmayr, "A 6b 600MHz 10mW ADC array in digital 90nm CMOS", *IEEE Solid-State Circuits Conference*, vol. 1, pp. 264-547, 2004.
- [8] Christian Vogel, "The Impact of Combined Channel Mismatch Effects in Time-Interleaved ADCs", *IEEE Transactions on Instrumentation and Measurement*, vol. 54, pp. 415-427, 2005.
- [9] Francesco Zanini, "Study of Generation of Distortion Harmonics Caused by Mismatches in Parallel ADC Architecture and suitable Solutions", National University of Ireland, 2006.
- [10] J. Elbornsson et al., "Analysis of Mismatch Noise in Randomly Interleaved ADC system", *Proc. IEEE ICASSP*, vol. 6, pp. 270-80 vol.6, 2003.
- [11] Y.C. Jenq, "Digital Spectra of Nonuniformly Sampled Signals: Fundamentals and High-Speed Waveform Digitizers", *IEEE Transactions on Instrumentation and Measurement*, vol. 37, pp. 245-251, 1988.
- [12] Christian Vogel et al., "Spectral Shaping of Timing Mismatches in Time-Interleaved Analog-to-Digital Converters", *IEEE Int. Symp. Circuits Sys.*, vol. 2, pp. 1394-1397, 2005.