Adaptive CADC Optimisation, Modelling and Testing

A.A. Platonov, Ł.M. Małkiewicz, K. Jędrzejewski

Warsaw University of Technology, Institute of Electronic Systems,
Nowowiejska 15/19, 00-665 Warsaw, Poland,
Tel. (48-22) 660-79-52, fax: (48-22) 825-23-00
E-mail: plat@ise.pw.edu.pl, lmalkiew@elka.pw.edu.pl, kala@ise.pw.edu.pl

Abstract. **–** Analytical approach to optimization, analysis, modeling and testing of the adaptive cyclic (sub-ranging) analog-to-digital converters (CADC) is considered. The particularity of the approach is digital computing the estimates (codes) of the input signal samples using optimal signal - processing algorithm. Upper boundaries for resolution, speed of conversion, and information characteristics are determined. Methodic of advanced CADC model-based simulation investigations is presented. The efficiency of simulation experiments as reliable, convenient and low-cost tool significantly simplifying and accelerating the search for optimal variants, design and analysis of CADC is shown.

1. Introduction

Quickly growing requirements for the speed and accuracy of conversion under general tendency to diminish the size, cost and power consumption of ADC are best satisfied in cyclic ADCs [1-3]. In works [4-10], a new concept of sub-optimal adaptive CADC is developed. Its particularity is refusal from the binary storing, shifting, adding, etc., elements for the codes of input samples forming [1-3], and their digital calculation using adaptive algorithms based on approach presented in [11]. The codes computing can be performed by the specialised computing high-bit block (in realisation of CADC as independent unit) or directly in the processor employing CADC as the analogue input.

Particularity of new conversion algorithm is that it is constructed as the result of concurrent optimization of the CADC's hardware and software [4-9], and realizes simultaneous calculation of the codes of estimates and adjusting of the analogue part of the converter. Simulation tools developed using theoretic results, permit the designers to obtain all main information necessary to build close-to-optimal (best under given conditions, sub-optimal) CADC. Such converters utilize completely resources of the hardware and software to improve the quality and speed of conversion to extent values. The most efficient way of CADC realisation is its integration with the microprocessor employing it as the analogue input. In this case, computing of estimates is realised directly in microprocessor that permits to omit the phase of intermediate sample codes computing and exclude redundant computing digital elements.

Different series of advanced experiments presented in [4-9] have shown high qualitative and quantitative accordance of simulations and theoretic results. Moreover, simulations give exhaustive answers on analytically unsolvable questions arising in CADC design. Among the other, theoretic and simulation tools developed in [4-9] create possibilities to analyse in details the problem of reliability of the simulation results, as well as more general task of reliability of the CADC testing procedures.

2. Mathematical description and optimization of CADC work

Principles of functioning, performance and benefits of sub-optimal CADCs are discussed in [4-10]. For the goals of the paper, it is enough to consider these questions using a block-diagram of CADC (Fig. 1). The input signal V_t is sampled in the sample-and-hold (S&H) block. Conversion of each sample $V^{(m)}$, ($m = 1,2...$) is performed in $n = T/\Delta t_0$ cycles independently from results of conversion of the previous sample ($T = 1/2F$ is sampling interval, $\Delta t_0 = 1/F_0$ is the duration of a single conversion cycle).

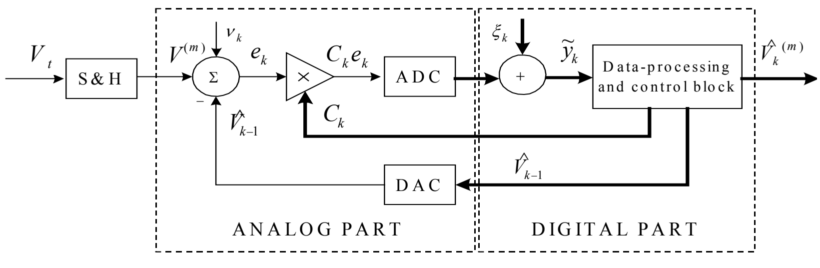

Figure 1. General structure of adaptive sub-optimal CADC with digital block of estimates computing.

During each interval T, the S&H block maintains the constant voltage V (index m is further omitted) at the first input of the summer Σ. For each cycle $k = 1,...,n$, summer forms the residual signal $e_k = V - \hat{V}_{k-1} + v_k$ routed to the input of digitally controlled or switched amplifier. The value $\hat{V}_{k-1}$ in e_k is the analogue equivalent of a digital estimate of the sample computed in data-processing block in previous cycle. Variable v_k describes the summary noise of the S&H block, feedback and the summer.

Amplified residual signal $C_k e_k$ is routed to the input of internal fast and low-bit A/D converter $\mathrm{ADC_{In}}$. Formed by $\mathrm{ADC_{In}}$, code $\tilde{y}_k$ is routed to the processing block, which computes new estimate $\hat{V}_k$ according to the recursion

$$\hat{V}_k = \hat{V}_{k-1} + L_k \tilde{y}_k; \quad (k = 1,...,n). \tag{1}$$

Estimate $\hat{V}_k$ is written into the memory unit instead of previous estimate and, simultaneously, is sent through the feedback $\mathrm{DAC_{In}}$ to subtracting block Σ, and new cycle of conversion begins.

Taking into account the always limited full-scale range (FSR) of $\mathrm{ADC_{In}}$ denoted further as $[-D, D]$, digital samples $\tilde{y}_k$ at $\mathrm{ADC_{In}}$ output can be presented by the model:

$$\tilde{y}_k = \begin{cases} C_k e_k + \xi_k & \text{for } C_k \,|e_k| \le D; \\ D sign(e_k) + \xi_k & \text{for } C_k \,|e_k| > D, \end{cases} \tag{2}$$

where ξ_k describes the quantization noise. The variance σ_ξ^2 of quantization noise is evaluated by commonly used formula: $\sigma_\xi^2 = \Delta^2/12 = D^2 2^{-2N_{ADC}}/3$, where N_{ADC} is the $\mathrm{ADC_{In}}$ resolution. The gains C_k and L_k in (1), (2) are mutually connected. Their values are determined by the designers, and determine the quality of estimates. For each $k = 1,...,n$, the closest-to-optimal (sub-optimal) gains C_k, L_k values are determined by formulas [4-7,11]:

$$C_k = \frac{D}{\alpha\sqrt{\sigma_v^2 + P_{k-1}}}, \quad L_k = \frac{C_k P_k}{\sigma_\xi^2 + C_k^2 \sigma_v^2} \tag{3}$$

where

$$P_k = \left(1 + \frac{C_k^2 P_{k-1}}{\sigma_\xi^2 + C_k^2 \sigma_v^2}\right)^{-1} P_{k-1} = (1+Q^2)^{-1} \left(1 + \frac{\sigma_v^2 Q^2}{\sigma_v^2 + P_{k-1}}\right) P_{k-1} \quad . \tag{4}$$

In these formulas, parameter

$$Q^2 = \frac{C_k^2 E(e_k^2)}{\sigma_\xi^2} = \frac{P_{sign}}{P_{noise}} = \left(\frac{D}{\alpha\sigma_\xi}\right)^2 = \frac{3}{\alpha^2} 2^{2N_{ADC}} \tag{5}$$

is the decimal signal-to-noise ratio (SNR) at the $\mathrm{ADC_{In}}$ output. Saturation factor α satisfies the equation $2\Phi(\alpha) = 1 - \mu$, where $\Phi(\alpha)$ is gaussian error function. Formula (4) determines MSE of conversion, minimal for the set of gains C_k, L_k under probability of internal $\mathrm{ADC_{In}}$ overloading not greater than a given small value μ. The initial conditions for recursions (1), (4) are: $\hat{V}_0 = V_0$; $P_0 = \sigma_0^2$.

According to (3)-(5), effective number of bits (ENOB) of estimates formed by sub-optimal adaptive CADC depends on the number of cycles as follows [8]:

$$N_k = \log_2\left(\frac{FSR}{2\Delta V_k}\right) = \log_2\left(\frac{FSR}{2\alpha\sqrt{P_k}}\right) = \frac{1}{2}\log_2\left(\frac{\sigma_0^2}{P_k}\right) \quad . \tag{6}$$

In (6), it is taken into account that FSR of the converter is determined as the interval [$-V_{\max}$, $V_{\max}$] = [$V_0 - \alpha\sigma_0$, $V_0 + \alpha\sigma_0$] which contains, with probability 1-μ, all possible values of the input samples. Similarly, one can check that the absolute error of estimates after k cycles has the value $\Delta V_k = \pm\alpha\sqrt{P_k}$ with probability not less than 1-μ [8]. In this case, the number of discrete values of the input signal resolved with a probability not less than 1-μ, is equal to $M_k = \Delta V_{\max}/\alpha\sqrt{P_k} = \sigma_0/\sqrt{P_k}$. Number of bits necessary for unambiguous presentation of each estimate from this set is equal to $N_k = \log_2 M_k$ that gives another interpretation of CADC resolution or ENOB.

In each CADC, power of the analogue noise v_k satisfies the inequality $\sigma_v^2 << \sigma_0^2$. Then, in the interval $1 \le k < n^*$ where $P_k >> \sigma_v^2$, MSE of estimates diminishes *exponentially* [4-11], and ENOB grows *linearly*, with maximal rate:

$$P_k = P_{k-1}(1+Q^2)^{-1} = \sigma_0^2(1+Q^2)^{-k}\ ;\ N_k = \frac{k}{2}\log_2\left(1 + \frac{3}{\alpha^2}2^{2N_{ADC}}\right) \quad , \tag{7}$$

respectively. Formulas (7) determine the lower and the upper boundaries of possible values of MSE and ENOB of estimates in interval $1 \le k < n^*$. For $k > n^*$ MSE and ENOB change accordingly much more slowly, as the hyperbolic and logarithmic functions of k, respectively. The point n^*:

$$n^* \approx \frac{1}{\log\ (1+Q^2)} \log\ \left(\frac{\sigma_0^2}{\sigma_v^2}\right), \tag{8}$$

determines the number of cycles necessary for the conversion accuracy to reach the values of the order of $\pm\alpha\sigma_v$ and for equation $P_{n^*} = \sigma_v^2$ to be fulfilled. Value n^* is the *optimal moment* to finish a sample conversion. Denoting MSE and ENOB of final output estimates $\hat{V}_{out} = \hat{V}_{n^*}$ as σ_{out}^2 and N_{out}, respectively, and taking nto account that $P_{n^*} = \sigma_{out}^2 = \sigma_v^2$, one can write:

$$N_{out} = \log_2\left(\frac{FSR}{2\alpha\sigma_{out}}\right) = \frac{1}{2}\log_2\left(\frac{\sigma_0^2}{\sigma_v^2}\right) = 1.661\, SNR_{0ut}\ , \quad \text{where} \quad SNR_{0ut} = 10\log_{10}\left(\frac{\sigma_0^2}{\sigma_v^2}\right). \tag{9}$$

Formula (9) determines final resolution of sub-optimal CADC, its connection with signal-to-noise ratio at the converter output, and coincides with the initial definition of ENOB of A/D converters given in IEEE Standards 1057-1994 and 1241-2000.

3. Some properties of sub-optimal CADC

Substituting (3), (4) into (6), one can obtain that resolution (ENOB) of sub-optimal adaptive CADC grows with a number of cycles as follows:

$$N_k = N_{k-1} + \frac{1}{2}\log_2\left(1+\frac{C_k^2 P_{k-1}}{\sigma_\xi^2 + C_k^2\sigma_v^2}\right) = N_{k-1} + \frac{1}{2}\log_2(1+Q^2) - \frac{1}{2}\log_2\left(1+Q^2\frac{\sigma_v^2}{\sigma_v^2+P_{k-1}}\right). \tag{10}$$

Under assumption that ADC_{ln} resolution $N_{ADC} \geq 4$ bit and $\alpha \geq 4$, value $Q^2 >> 1$. Then, in the interval $1 \leq k < n^*$, current values of N_k increases linearly according to the relationship:

$$N_k = \frac{k}{2}\log_2(1+Q^2) = k\left(N_{ADC} - \frac{1}{2}\log_2\frac{\alpha^2}{3}\right) = k\ (N_{ADC} - \log_2\alpha\ + 0.7925)\ \text{[bits]}, \tag{11}$$

which determines the upper boundary of ENOB, i.e. resolution of CADC for $1 \leq k < n^*$. For $k > n^*$, where $P_k < \sigma_v^2$, ENOB depends on the number of cycles logarithmically.

For $\Delta t_0 = 1/F_0$ and $T = 1/2F$, the number of cycles of the sample conversion can be presented as ratio $n = T/\Delta t_0 = F_0\ /2F$. If each sample is converted in the optimal number of cycles n^*, formula (8) gives:

$$F\log\left(\frac{\sigma_0^2}{\sigma_v^2}\right) = \frac{F_0}{2}\log\left(1+\frac{P_{sign}}{P_{noise}}\right) = \frac{F_0}{2}\log(1+Q^2), \tag{12}$$

where $P_{sign}/P_{noise} = (D/\alpha)^2/\sigma_\xi^2 = Q^2$. Relationship (12) expresses well known in information and signal processing theory the SNR-to-bandwidth trade-off.

Information $I(V;\tilde{y}_1^k)$ about the samples V in observations $\tilde{y}_1^k = (\tilde{y}_1,...,\tilde{y}_k)$, according to definition, is equal to uncertainty removed by observations, i.e. difference between the prior $H(V)$ and posterior $H(V\,|\,\tilde{y}_1^k)$ entropies of the input signal samples: $I(V,\tilde{y}_1^k) = H(V) - H(V\,|\,\tilde{y}_1^k)$. In the gaussian case, $I(V;\tilde{y}_1^k)$ has the value [7,8]:

$$I(V,\tilde{y}_1^k) = \frac{1}{2}\log_2\left(\frac{\sigma_0^2}{P_k}\right)\ \text{[bit]} \tag{13}$$

that coincides with expression (6) for ENOB and represents the mean number of bits necessary for the binary presentation of input samples V with the accuracy $\pm\alpha\sqrt{P_k}$.

If the gains C_k and L_k increase according to (3), the information flow $R_{out} = I(V,\tilde{y}_1^k)/T = N_{out}/T$ at CADC output reaches, for each $1 \leq k < n^*$, the maximal value:

$$R_{out} = \frac{F_0}{2}\log_2\left(1+\frac{P_{sign}}{P_{noise}}\right) = \frac{F_0}{2}\log_2\left(1+\frac{3}{\alpha^2}2^{2N_{ADC}}\right) = F_0(N_{ADC} - \log_2\alpha + 0.7925)\ \text{[bit/s]}\ . \tag{14}$$

Greater information flow through the analogue part to data-processing block of CADC under given probability of saturation is impossible. Thus, (14) determines information capacity of CADC. Let us note that the left side of (14) coinsides with Shannon's formula for capasity of Gaussian channel [12]. Equality of the rate of information trasmission to the capacity of CADC proves full utilization of the resources of its analogue and data-processing parts.

The equality of discrete and continuous sets of digital estimates permits us to consider DAC_{ln} as the quantizer of continuous digital signals into discrete analogue ones. Assuming the analogue quantization noise is greater than other analog noises, we may evaluate its power by standard formula $\sigma_v^2 = \Delta_{DAC}^2/12 = (\alpha\sigma_0 2^{-N_{DAC}})^2/3$. For $Q^2 >> 1$, one can get the following, useful for engineering calculations, approximate formulas for upper values of resolution and speed of conversion (as the number of cycles per sample):

$$N_{out} = \frac{1}{2}\log_2\left(\frac{\sigma_0^2}{\sigma_v^2}\right) = N_{DAC} - \log_2\left(\frac{\alpha}{\sqrt{3}}\right)\quad ; \qquad n_{opt} = \frac{N_{DAC} - \log_2(\alpha/\sqrt{3})}{N_{ADC} - \log_2(\alpha/\sqrt{3})}\ . \tag{15}$$

The theory also permits to evaluate the dependence of MSE and ENOB on non-adequate CADC application, as well as on the noises and errors in the parameters of the analogue part and algorithm setting. For instance, following relationship can be obtained which determines the increment of MSE caused by difference between the "nominal" parameters - which CADC or input signal and noises should or are assumed to have, and their actual values - on $\Delta V_0 = \bar{V}_0 - V_0$; $\Delta\sigma_0^2 = \bar{\sigma}_0^2 - \sigma_0^2$; $\Delta\sigma_\nu^2 = \bar{\sigma}_\nu^2 - \sigma_\nu^2$:

$$\bar{P}_k = P_k + \left(\frac{P_k}{P_0}\right)^2 \left\{ \Delta\sigma_0^2 + (\Delta V_0)^2 + \Delta\sigma_\nu^2 \sum_{i=1}^{k} \left(\frac{Q^2 P_0}{(1+Q^2)\sigma_\nu^2 + P_{k-1}} \right)^2 \right\} . \qquad (16)$$

Substituting (16) into (8), one can easily find a corresponding relationship for the increment of ENOB:

$$\bar{N}_k = N_k - \frac{1}{2}\log_2 \left\{ 1 + \frac{P_k}{P_0} \left[\frac{\Delta\sigma_0^2 + (\Delta V_0)^2}{P_0} + \Delta\sigma_\nu^2 \sum_{i=1}^{k} \left(\frac{Q^2}{(1+Q^2)\sigma_\nu^2 + P_{k-1}} \right)^2 \right] \right\} . \qquad (17)$$

One should add that each estimate $\hat{V}_k$ of each input value V calculated according to (1)-(5) has the initial bias:

$$E(\hat{V}_k \mid V) = V + P_k P_0^{-1} (V_0 - V), \qquad (18)$$

that is a general property of all Bayesian estimates. The bias quickly disappears due to the fast transition from prior value V_0 to the more and more accurate estimate $\hat{V}_k$ of the input sample value V.

4. Full scheme of CADC simulation analysis

Initially, the objective of simulations was a verification of theoretic results and analysis of particularities of CADC functioning [4-9]. It was established that the most efficient way of CADC simulation analysis is a registering of the changes in MSE and ENOB *trajectories* (dependencies $\hat{P}_k = \hat{P}(k)$ and $\hat{N}_k = \hat{N}(k)$ on the number of cycles) depending on the changes of the analyzed parameters or characteristics. Empirical trajectories values of MSE $\hat{P}_k$ and ENOB $\hat{N}_k$ were calculated using blocks of estimates $\hat{V}_k^{(m)}$ of the samples $V^{(m)}$ ($m = 1,...,M$) of the input signal, according to formulas:

$$\hat{P}_k = \frac{1}{M}\sum_{m=1}^{M}\left[V^{(m)} - \hat{V}_k^{(m)} \right]^2 ; \qquad \hat{N}_k = \frac{1}{2}\log_2\left(\frac{\sigma_0^2}{\hat{P}_k}\right) \qquad (19)$$

Analysis of collected results allowed us to choose the most convenient, reliable and universal methods of the analysis of different aspects of CADC work, and organize them into ordered set of relatively independent groups of experiments each answering its own set of questions. The systematization was performed in the way enabling concurrent performance of similar experiments with laboratory prototypes or production versions of CADC. The experiments were joined into following groups:

1. Direct analysis of characteristics of the "ideal" (built strictly according to theoretic results) sub-optimal CADC. The changes of trajectories $\hat{P}_k = \hat{P}(k)$ and $\hat{N}_k = \hat{N}(k)$ are measured depending on the values of the parameters V_0, σ_0^2 of input signal, on saturation factor α; on the parameters of the analogue part N_{ADC}, $[-D, D]$; N_{DAC} and variances σ_ν^2, σ_ξ^2 of noises including methods of their evaluations.
2. Analysis of consequences of a non-adequate application of CADC. The changes of MSE and ENOB trajectories are measured depending on differences between the "nominal", used in the conversion algorithm , and "real" values of the parameters of the input signal. The influence of differences $\Delta V_0 = \bar{V}_0 - V_0$ and $\Delta\sigma_0^2 = \bar{\sigma}_0^2 - \sigma_0^2$ was analyzed, as well as of different classes of input signals: white gaussian noise, sin-wave; deviations from gaussian form of distribution $p_0(V)$.
3. Analysis of influence of implementation errors. The manufacturing errors were considered as differences between the "nominal" and real values of parameters of the analogue part. Following errors were analyzed: non-ideality of quantizer transfer function, presence of input offset $\Delta V_0 = \bar{V}_0 - V_0$, errors in gains setting $\Delta C_k = \bar{C}_k - C_k$, form of ADC_{In} characteristic (mid-raiser or mid-tread); ADC_{In} and DAC_{In} characteristic errors (differential and integral nonlinearity, input/output offsets); errors in evaluation of variances σ_ξ^2 and σ_ν^2, and temperature drifts of the parameters.
4. Analysis of MSE and ENOB trajectories changes depending on differences between the "nominal" and real values of the parameters of data-processing algorithm in cases of its simplification or modification.
5. Complex investigation of the fields and conditions of the parametric tolerance and stability of optimal CADCs depending on parameters of the input signal $\bar{V}_0$, $\bar{\sigma}_0^2$ and α, of analog part $\bar{V}_k$, $\bar{C}_k$, N_{ADC}, N_{DAC}; power of noises $\bar{\sigma}_\nu^2$, $\bar{\sigma}_\xi^2$; on the gains $\bar{L}_k$ values; on the form and distribution of the signal.
6. Comparison of different variants of possible CADC realization and choice of the most suitable variant.
7. Comparison of different variants of optimal CADC with existing non-optimal CADC or other ADCs.
8. Analysis of the testing methodic and signal influence on results of CADC performance evaluations.
9. Support of the laboratory experiments with hardware prototypes of CADC (calculation, storing and visualization of theoretic and experimental results, analysis of the sources of their disagreement).

Apart from MSE and ENOB, simulations were used for evaluation and analysis of information capacity of CADC, output signal-to-noise ratio, changes in spectra of output signal, frequency characteristics of CADC (THD, SINAD, etc.). The results of experiments had confirmed the efficiency and usefulness of simulations as an additional analytical tool in CADC analysis and design.

5. Some results of CADC simulation analysis

The software for simulation analysis of CADC functioning and design consists of a digital signal generator, full mathematical model of CADC and data processing modules. The analogue part module is designed taking into account the step-wise form of the input-output characteristic and finite input range of ADC_{In}. Digital part of CADC is modelled directly on the basis of algorithm (3)-(5). Signal generator module generates digital sequences of the samples of following test-signals: a) sin-wave; b) gaussian and c) uniformly distributed white noise. There is assumed that duration of each sample permits the CADC to perform *n* cycles of conversion.

All the experiments were followed by calculation of corresponding theoretic dependencies next compared with the measured ones. The results of investigations are presented in [4-9] and other works. At present, we have qualitative and quantitative answers on all main questions listed in Sect. 3 in groups 1-4 and, partially, in groups 5-9.

Below, some of the new results of simulations, important for design and further investigations are presented. Calculations of trajectories of MSE $\hat{P}_k$ and ENOB $\hat{N}_k$ were carried out according to (19) using blocks of M=1000 estimates $\hat{V}_k^{(m)}$ ($m=1,...,M$) obtained by application of algorithm (1)-(5) for each $k=1,...,n$ using realisations of the signal $y_k^{(m)}=V^{(m)}+v_k$, ($m=1,...,M$) where values V_k are gaussian random values with zero mean and variance $\sigma_0^2=6.25\cdot 10^{-2}$. Other parameters were taken as follows: $D=1.25$, $\sigma_v^2=10^{-8}\sigma_0^2$; $\sigma_\xi^2=D^2 2^{-2N_{ADC}}/3$, α=5, (μ=10^{-7}).

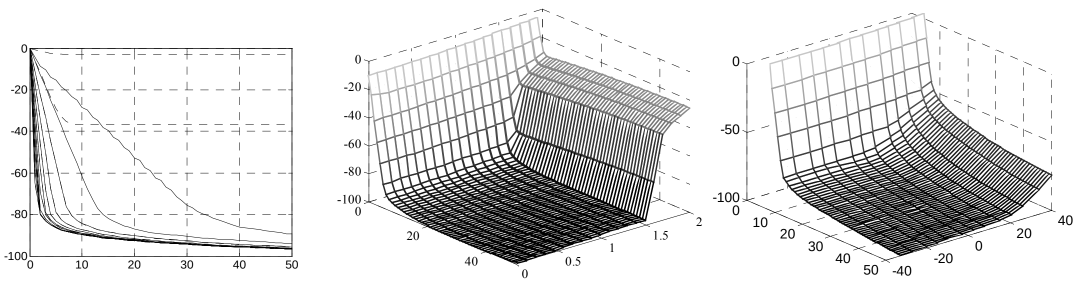

Figure. 2. Changes in trajectories of empirical MSE depending on: (a) - resolution of ADC_{In} with the mid-tread and mid-riser characteristics; (b) - ratio of the nominal to real power of the input signal ($a=\bar{\sigma}_0/\sigma_0$); (c) - ratio $a=20\log_{10}(\bar{\sigma}_v/\sigma_v)$ of the nominal and real power of the analogue noise v_k.

Plots in Fig. 2a show the influence of ADC_{In} resolution on MSE of conversion. Continuous lines refer to CADC built using ADC_{In} with a transition function of the mid-riser type, dashed lines refer to CADC with ADC_{In} of the mid-tread type. Experiments were carried out for $N_{ADC}=1\div 12$, corresponding plots in Fig. 2a are ordered from the top to the bottom. The results show that difference between the ADC_{In} characteristics does not influence MSE beginning with $N_{ADC}=3$.

In analysis of non-adequate application of CADC, it was established that differences between the actual $\bar{V}_0$ and nominal V_0 mean values of the signal in limits less than $\pm 0.5\sigma_0$ do not change the MSE. Similarly, MSE $\hat{P}_k$ has a wide interval of insensitivity to the differences between the nominal and actual variances of the signal $\Delta\sigma_0^2=\bar{\sigma}_0^2-\sigma_0^2$. Typical plot of MSE trajectories is presented in Fig. 2b, ($\bar{V}_0, V_0=0$; N_{ADC}=4). Dependence of MSE on discrepancies between the actual $\bar{\sigma}_v^2$ and nominal σ_v^2 values of analog noise power is weak (see Fig. 2c), which can be used in CADC adjusting. Growth of MSE in Figs. 2b,c for greater discrepancies is caused by increasing probability of ADC_{In} saturation.

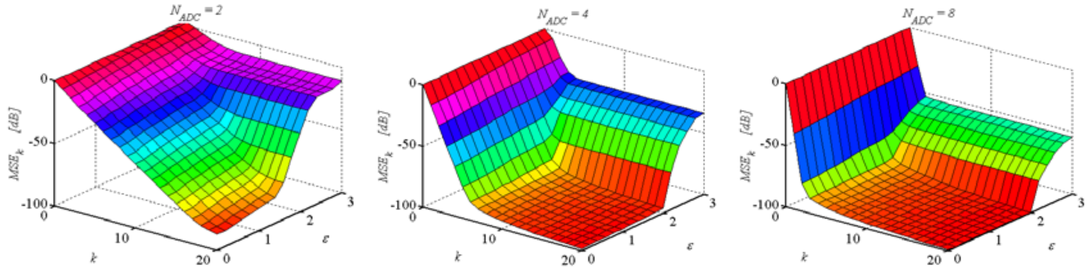

Figure 3: Empirical MSE as a function of DNL errors intensity ε for different $N_{ADC} = 2, 4, 8$.

The last group of results to present concerns the influence of ADC_{In} transition function differential nonlinearity (DNL). The errors of quantisation levels setting were modelled as random displacements uniformly distributed in interval $[-\varepsilon\,\Delta/2,\ \varepsilon\,\Delta/2]$, where parameter ε determines the variance of errors (errors intensity). Increase of DNL ($\varepsilon > 1$) causes the appearance of overlapping and missing codes. The plots for MSE trajectories depending on the parameter ε obtained under different N_{ADC} are presented in Fig. 3. The results also show a wide interval of insensitivity of CADC to errors in ADC_{In} quantization levels setting, which extends slowly with N_{ADC} enlargement.

6. Conclusions

The sub-optimal CADCs built on the basis of the solution of optimization task, fully utilize the resources of their analogue part and software. This makes these converters the most efficient, simplest and least expensive devices among the set of possible versions of CADCs of the same predestination. Expressions for achievable resolution, speed of conversion and information capacity enable designers to determine the conditions ensuring CADC performance close to these boundaries.

The developed formalism was used to design the efficient and universal model-based methodic of CADC simulation analysis. Joint application of theory and simulations may reduce significantly the cost and time of analysis and adjustment of the laboratory and pre-manufacturing prototypes of CADC. Simultaneously, it may improve and make the results of analysis and testing more reliable.

Main fields of results of the paper application are: the decision making on pre-design stage, support of the laboratory researches, evaluation of expected performance, verification of calibration and testing procedures.

References

[1] Maloberti F., High-speed data converters for communication systems," *IEEE Circuits and Systems Magazine*, vol. 1, No. 1, First Quarter 2001, pp. 27-36.

[2] Robert C., Grisoni L., Heubi A., Balsiger P., Pellandini F., "Micro power high-resolution A/D converter," *Proc. of Int. Conf. ICSAP'99,* Orlando, Sept. 1999.

[3] Goodenough F., Next-generation 12-, 14-bit IC ADCs sample signals, *Electronic Design,* v. 37, No. 4, Penton Publishing, Cleveland, OH, US, 1989, pp. 121-123.

[4] Platonov A., Jędrzejewski K., Jasnos J.,Design and analysis of algorithmic multi-pass A/D converters with theoretically highest resolution and rate of conversion, *Measurement,* vol. 30, No. 3, 2004, pp. 267-278.

[5] Platonov A., Malkiewicz Ł.M., Analytical methods in high-performance cyclic A/D converters design, *Europ. Conf, on Circuit Theory and Design ECCTD 2003,* Kraków, Poland, Sept. 2003, pp. 189-192.

[6] Platonov A.A., Małkiewicz Ł.M, Analytic design of cyclic low energy ADC with sub-optimal estimates calculation, *IMEKO XVII World Congress,* Dubrovnik, Croatia, June 2003, pp. 141-146.

[7] Platonov A.A., Jędrzejewski K., Improvement of cyclic A/D converters performance under greater number of conversion cycles, *Europ. Conf. on Circuit Theory and Design ECCTD'2003,* Kraków, Poland, 1-4 Sept. 2003, pp. 193-196.

[8] Jasnos J., Platonov A.A., The hardware prototype of intelligent cyclic A/C converter, *Proc.of Polish-Czech-Hungarian Workshop on Circuit Theory and Sign. Proc.* Prague, Czechia, Sept. 2003, pp. 25-30.

[9] Platonov A.A., Optimal design of adaptive cyclic ADC, *Proc. of 2nd IEEE Int. Conf. on Circuits and Systems for Communication, ICCSC 2004,* Moscow, Russia, June 30-July 2, 2004.

[10] Platonov A.A. "Multi-Pass Analog-Digital Converter", Int. Patent Application No. PCT/PL03/00041, *Publ. WIPO*, 30.10.2003.

[11] Platonov A.A., "Optimal identification of regression-type processes under adaptively controlled observations," *IEEE Trans. on Sign. Proc.*, vol. 42, No.9, pp. 2280-2291, Sept.1994.

[12] Gallager R., *Information theory and reliable communication,* J.Wiley, New York, 1968.