Stochastic Test of 24bit-AD Converter – Case Study

Jan Holub, Josef Vedral

Czech Technical University, Faculty of Electrical Engineering, Dept. of Measurement, Technicka 2, 166 27 Prague 6, Czech Republic, Phone: +420-22435-2131, fax: +420-23333-9929, e-mail: holubjan@feld.cvut.cz

Abstract- Effective number of bits (ENOB) and normality test of code word histogram of Micro-Converter ADUC824 has been evaluated at the FEE CTU Prague and the methodology and results are shown and discussed in the paper.

I. ADUC824 Characteristics

The Data Acquisition System is based in Micro-Converter ADUC834. The ADuC834 is a complete smart transducer front end, integrating two high resolution ADCs, an 8-bit MCU, and program/data Flash/EE memory on a single chip. The two independent ADCs (primary and auxiliary) include a temperature sensor and a PGA (allowing direct measurement of low-level signals). The ADCs with on-chip digital filtering and programmable output data rates are intended for the measurement of wide dynamic range, low frequency signals, such as those in weigh scale, strain-gage, pressure transducer, or temperature measurement applications. The device operates from a 32 kHz crystal with an on-chip PLL generating a high frequency clock of 12.58 MHz. This clock is routed through a programmable clock divider from which the MCU core clock operating frequency is generated. The micro-controller core is an 8052 and therefore 8051 instruction set compatible with 12 core clock periods per machine cycle. 62 Kbytes of nonvolatile Flash/EE program memory, 4 Kbytes of nonvolatile Flash/EE data memory, and 2304 bytes of data RAM are provided on-chip. The program memory can be configured as data memory to give up to 60 Kbytes of NV data memory in data logging applications.

The unit contains also two programmable gain differential analogue input channels. The gain ranges from 1 to 128 allowing the device to accept unipolar signal between 0 to + 20 mV to 0 to + 2,56 V or bipolar signals in the range from ± 20 mV to ± 2,56 V using + 2,5 V reference input voltage.

The input signal at the selected analogue input channel is continuously sampled at a rate determined by the frequency of the master clock.

The programmable gain function on the analogue input is also incorporated in this $\Sigma-\Delta$ modulator with the input sampling frequency being modified to give the higher gains. A digital low-pass filter processes the output of the $\Sigma-\Delta$ modulator and updates the output register at a rate determined by the first notch frequency of this filter.

II. ENOB Measurement

Measuring system for ADC Effective Number of Bits (ENOB) [1] determination has been developed. It consists of the DC voltage calibrator Fluke 5100B and signal generator Stanford Research DS360. Lower voltages are derived using passive divider based on manganine resistors, see Fig. 1.

The stochastic test method [2], [3] has been deployed on ADUC824 housed in portable reference device. Accordingly, 10^{11} samples would be necessary for histogram test of 24-bit ADC to achieve 5% confidence level of ENOB. Due to enormous number of samples required, the simplified method using measurement interpolation has been used (not all the code words have been covered by the test). Basic definition of ENOB as given in [1] is deployed:

$$ENOB = log_2 \frac{2^n}{RMS_{NOISE}\sqrt{12}} [LSB] \tag{1}$$

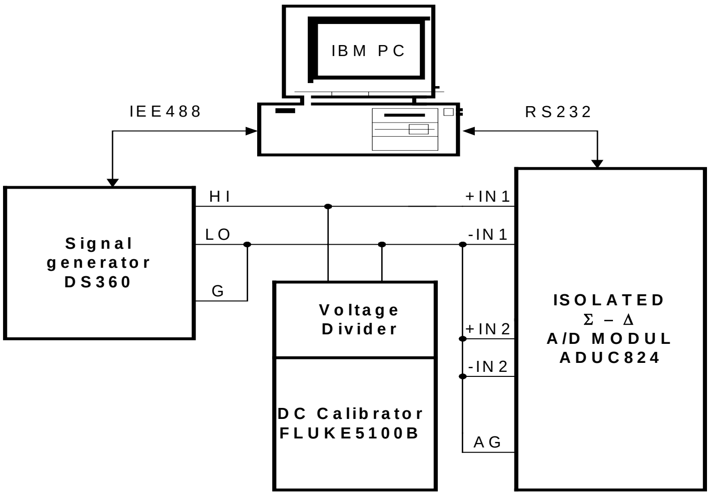


Figure 1 Measurement system for ENOB evaluation

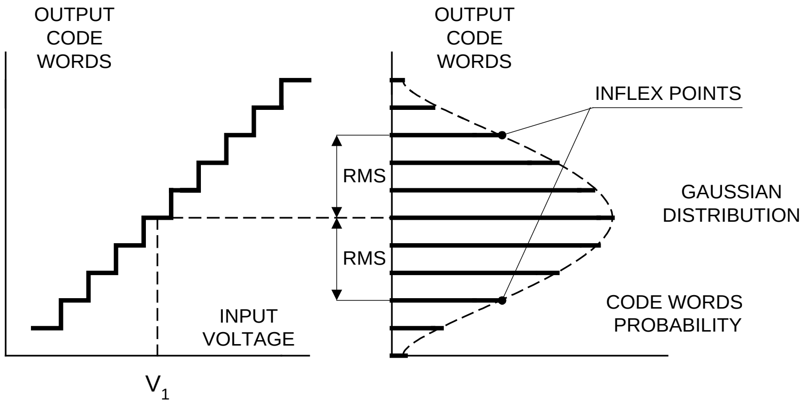
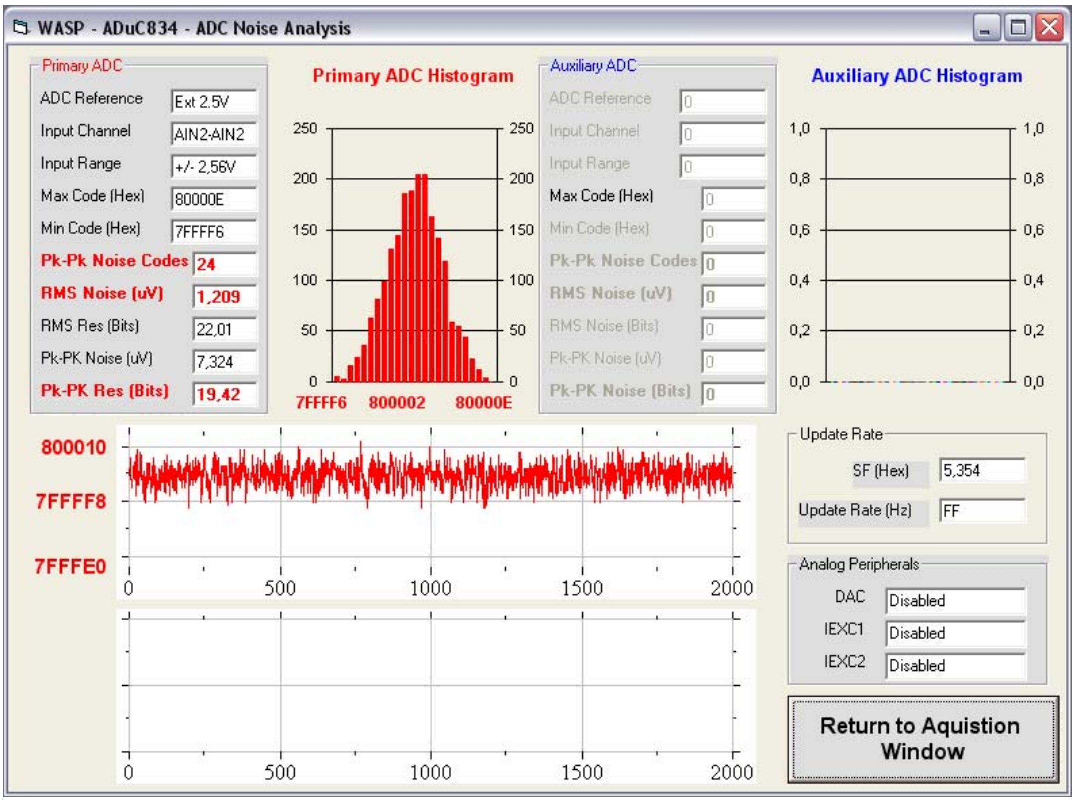


Figure 2 Code Words Histogram

Measured results of effective number of bits versus gain of input amplifier and stop frequency is presented in Tab.1.

Tab.1 Effective resolution of primary 24 bit ADC versus gain and sample rate

	Gain and ADC input range							
sample rate [Sa/s]	G = 1 2,56V	G = 2 1,28V	G = 4 640mV	G = 8 320mV	G = 16 160mV	G = 32 80mV	G = 64 40mV	G = 128 20mV
5,3	21.9	21.6	21.2	20.7	19.8	18.9	17.8	16.8
19,8	20.9	20.7	20.3	19.8	18.9	17.9	16.9	15.9
105,3	18.9	18.1	17.9	17.9	17.2	16.5	15.7	14.7



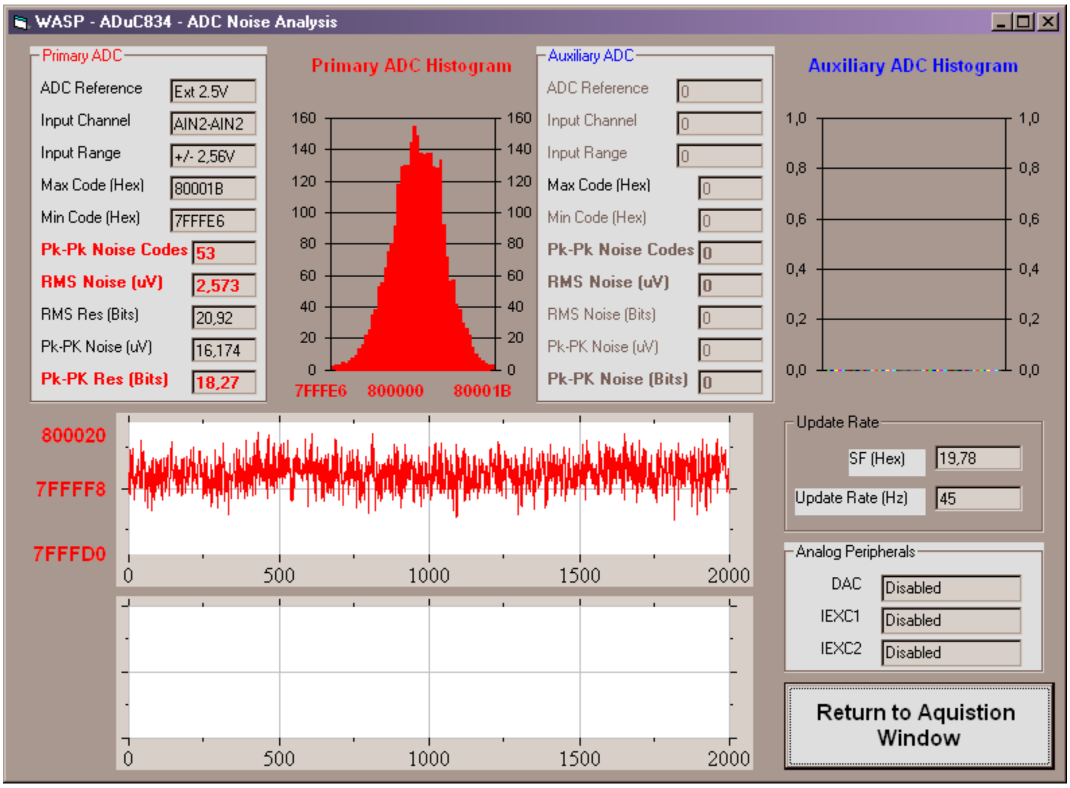
Primary ADC
ADC Reference: Ext 2.5V
Input Channel: AIN2-AIN2
Input Range: +/- 2,56V
Max Code (Hex): 80000E
Min Code (Hex): 7FFFF6
Pk-Pk Noise Codes: 24
RMS Noise (uV): 1,209
RMS Res (Bits): 22,01
Pk-PK Noise (uV): 7,324
Pk-PK Res (Bits): 19,42

Auxiliary ADC
ADC Reference: 0
Input Channel: 0
Input Range: 0
Max Code (Hex): 0
Min Code (Hex): 0
Pk-Pk Noise Codes: 0
RMS Noise (uV): 0
RMS Noise (Bits): 0
Pk-PK Noise (uV): 0
Pk-PK Noise (Bits): 0

Update Rate
SF (Hex): 5,354
Update Rate (Hz): FF

Analog Peripherals
DAC: Disabled
IEXC1: Disabled
IEXC2: Disabled

Figure 3 Example of test for sample rate 5 Sa/s



Primary ADC
ADC Reference: Ext 2.5V
Input Channel: AIN2-AIN2
Input Range: +/- 2,56V
Max Code (Hex): 80001B
Min Code (Hex): 7FFFE6
Pk-Pk Noise Codes: 53
RMS Noise (uV): 2,573
RMS Res (Bits): 20,92
Pk-PK Noise (uV): 16,174
Pk-PK Res (Bits): 18,27

Auxiliary ADC
ADC Reference: 0
Input Channel: 0
Input Range: 0
Max Code (Hex): 0
Min Code (Hex): 0
Pk-Pk Noise Codes: 0
RMS Noise (uV): 0
RMS Noise (Bits): 0
Pk-PK Noise (uV): 0
Pk-PK Noise (Bits): 0

Update Rate
SF (Hex): 19,78
Update Rate (Hz): 45

Analog Peripherals
DAC: Disabled
IEXC1: Disabled
IEXC2: Disabled

Figure 4 Example of test for sample rate 19.78 Sa/s

III. Conclusions

The decreasing trend of effective resolution for sample rates in range 5 Sa/s to 105,3 Sa/s and gains from 1 to 128 is evident. The maximal value of effective resolution is 20,6 bits for sample rate 5 Sa/s and gain 1 (voltage range 2,56 V). The minimal effective resolution is 14,2 bits for sample rate 105,3 Sa/s and gain 128 (voltage range 20 mV). The deviations of effective resolution for any gain and sample rate are less than 5%.

IV. Acknowledgements

This project is supported by the Grant Agency of the Czech Republic, GACR 102/01/D087.

REFERENCES

[1] IEEE Std 1241-2000, IEEE Standard for Terminology and Test Methods for ADC, The Institute of Electrical and Electronics Engineers, New York, 2000

[2] Holub, J.,Vedral, J.: Evaluation of Frequency Dependency of Effective Number of bits by means of Stochastic Testing Signal, 6th Europan Workshop on ADC Modelling and Testing, Lisboa,, September 2001

[3] Vedral, J., Holub, J.: Testing of High Resolution ADCs with Deterministic and Stochastic Signals, ETW03 Europan Test Workshop, Maastricht, May 2003