Non-linearity Correction of ADCs in Software Radio Systems

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Abstract **-** The paper presents the results of the experimental validation of a method for digital compensation of ADC non-linearity errors. First, the theory underlying the method is briefly described. Then, the compensation method has been validated both on sinusoidal signals and on 3rd generation mobile telecommunication signals, compliant to 3GPP specifications.

I. Introduction

In measurement and control systems, in which high-frequency signals are involved, both fast sampling and processing and high accuracy are required.
These requirements are particularly relevant in many applications related to signal interception and verification, such as electronic surveillance systems, military communications, emitters intercepting and interference identification. This kind of applications, in fact, is often realized by using software radio receivers [1].
A software radio is a radio system whose channel modulation waveforms are defined in software [2]. That is, the signals to be transmitted are generated as digital waveforms and then converted from digital to analog at base band or intermediate frequency (IF) via a wideband digital-to-analog-converter (DAC). Then, they are possibly upconverted from IF to RF and transmitted. The receiver, similarly, employs a wideband analog-to-digital-converter (ADC) that captures all the channels of the software radio node. The receiver, then, extracts, downconverts and demodulates the channel waveforms using software running on a general purpose processor or a Digital Signal Processor (DSP) [2].
In these systems the ADC characteristics play an important role in the definition of the quality of the communication. The receivers, in particular, require both a high sampling rate and a large dynamic range, because (i) the wideband IF signal should be sampled at a frequency high enough to include all the required channels, and (ii) the spurious free dynamic range (SFDR) should be high enough to ensure that some spurious spectral components with high amplitude do not hide the useful signal.
In this scenario, in order to improve the receiver performance, the identification of internal non-linearity errors of the ADC and the development of methods for their correction in real-time could achieve a considerable SFDR increase.
Several papers dealing with the real-time correction of ADC non-linearities can be found in literature. The most part of them achieves a dynamic compensation of non-linearity errors by using a phase-plane [3] or state-space [4] approach. In these cases, the difference between the actual and the ideal code is collected in a look-up table (LUT), as a two-dimensional function of the current output code, and either the slope of the signal or the previous code. This approach requires, however, a large amount of memory [5] in order to build up the LUT. Moreover, some problems arise with (i) the selection of the type and number of the calibration signals [6], and (ii) the compensation of small non-linearities, whose values are smaller than the quantization step.
An alternative approach to non-linearity reduction using bayesian filtering has been proposed in [7,8], tested in simulation and implemented on a DSP board equipped with a low frequency, high resolution ADC [9].
In order to prove the capability of the method in more realistic conditions, a test plan on a high frequency, low resolution ADC has been carried out.
The experimental tests have been divided in three phases. First, some tests have been carried out on a converter by using sine-wave signals to identify the capability of the method of compensating the intrinsic nonlinearity of the ADC, which is below the LSB [9]. A second group of tests has been

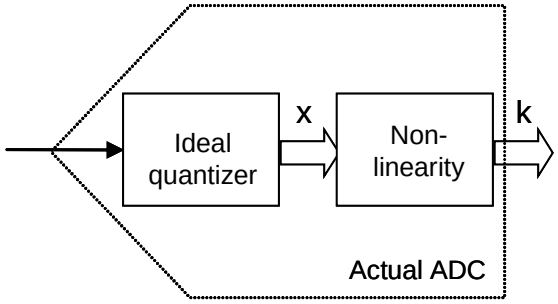

Figure 1. ADC model, used for deriving the correction method.

realized with sine-wave signals by introducing a self-built analog nonlinearity affecting few codes but with an amplitude of several LSBs and considering the ADC as ideal [9]. Finally, an experimental phase has been carried out with a new analog non-linearity, which occupies the whole full scale range of the ADC. During this phase sine waves and Universal Mobile Telecommunication System (UMTS) signals, based on the Wideband Code Division Multiple Access (W-CDMA) technique, have been used.
The first two phases already showed a relevant SFDR increase [9]. In the paper the results of the last phase are presented.
The method has been first validated on simulated W-CDMA signals. Then, it has been verified on a test bench consisting of a PC data acquisition board equipped with an 8-bit 1 GS/s A/D converter. In order to consider the ADC as an ideal one, a self-built analog distortion circuit, whose non-linearity is much greater than the intrinsic non-linearity of the ADC, has been used. In the next Sections the method is briefly recalled, then the results obtained by the simulation phase are given. Finally, the results of the characterization phase using actual signals are presented.

II. The method

For the scope of the present work, the effect of the non-linearity on an actual ADC has been modelled as a distorting channel in which the output of an ideal quantizer x is mapped to the actual output k (Fig.1) [8]. In this case, an estimation of the original code x can be obtained by the following formula [8]:

$$\hat{x} = E\{x \mid k\} = \sum_{x=0}^{2^N-1} x \cdot p(x \mid k), \tag{1}$$

where *E{}* is the expected value operator, *N* is the number of bits of the converter, *p(k)* and *p(x)* are the probabilities of the actual code *k* and the ideal one *x*, respectively. *p(x|k)* is the conditional probability of *x*, given *k*.
The conditional probability *p(x|k)* is obtained by means of the Bayes theorem, as follows:

$$p(x \mid k) = \frac{p(k \mid x) \cdot p(x)}{p(k)} = \frac{p(k \mid x) \cdot p(x)}{\sum_{x=0}^{2^N-1} p(x) p(k \mid x)}. \tag{2}$$

If dither is applied, in order to reduce quantization noise and small scale non-linearity errors, an estimate of the ideal code x can be found by over-sampling, applying a Bayesian filter and using a smoothing window of length $2L_s+1$ to remove the dithering:

$$\hat{x}[i] = \frac{1}{2L_s+1} \sum_{j=-L_s}^{L_s} x_e[i+j] = \frac{1}{2L_s+1} \sum_{j=-L_s}^{L_s} \sum_{x[i]=0}^{2^N-1} x[i] \frac{p(k[i+j] \mid x[i+j]) p(x[i+j])}{p(k[i+j])}. \tag{3}$$

In this case a simple rectangular smoothing window has been chosen [8].
The matrix containing *p(k|x)* conditional probabilities can be evaluated in a calibration phase starting

from the code transition levels as shown in [7]. Sine wave histogram test procedure, reported in [10], has been used for estimating code transition levels.

III. Simulation results

A simulation study has been carried out in MATLAB language on W-CDMA signals, according to the block scheme reported in Fig. 2. A W-CDMA signal is generated in compliance with 3GPP specifications [11] at an IF frequency of 10.32 MHz and double precision samples. Then, it is quantized using both an 8-bit ideal ADC model and an 8-bit actual ADC model, with a simple non-linearity 40 codes wide and 6 codes high, having the INL shown in Fig. 3.
After the quantization, the method for the non-linearity correction has been applied and the SFDR referred to the carrier frequency has been evaluated, as in [10]. Fig. 4 shows the Power Spectral Density (PSD) of the signal before and after the non-linearity correction, respectively. It can be noted a relevant improvement of more than 20 dB in the SFDR, referred to the carrier frequency.

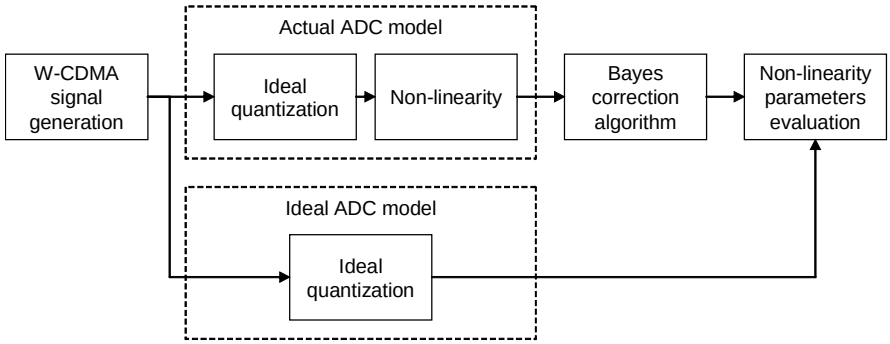

Figure 2. Block scheme of the procedure adopted for the simulation tests.

IV. Experimental results

The test bench consists of a development system composed of a PC based on a Pentium IV 1,7 GHz CPU and a Signatec PDA1000 data acquisition board, equipped with a 1 GS/s 8-bit flash ADC.
As it can be seen in Fig. 5, signals are generated by an Agilent E4438C vector signal generator, then, sent to a self-built analog board which is used for corrupting the signal with a known non-linearity. An electrical scheme of this circuit is given in Fig. 5 in enlarged view. Data are collected by the PC and corrected.
In a first phase, some experimental tests have been conducted using a 15 MHz sine-wave signal. The signal has been acquired using a 250 MS/s sampling frequency. The integral non-linearity (INL) has been evaluated by means of the sine-wave histogram test procedure [10]. From the INL diagram of Fig.6a the INL introduced by the non-linearity circuit can be clearly observed. Fig. 6b shows the results of the correction method. In particular, a reduction in the second harmonic of 28.8 dB can be observed, while the SINAD increase is equal to 23.52 dB.

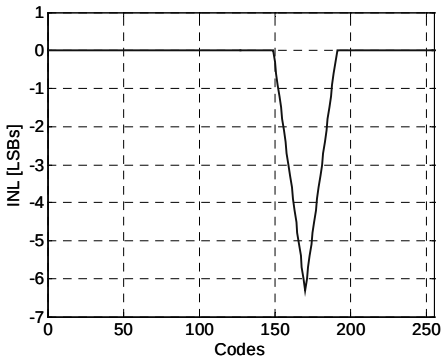

Figure 3. INL of the non-linearity model.

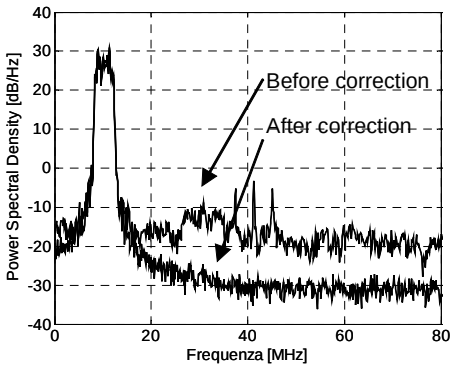

Figure 4. PSD of a W-CDMA signal before and after the correction.

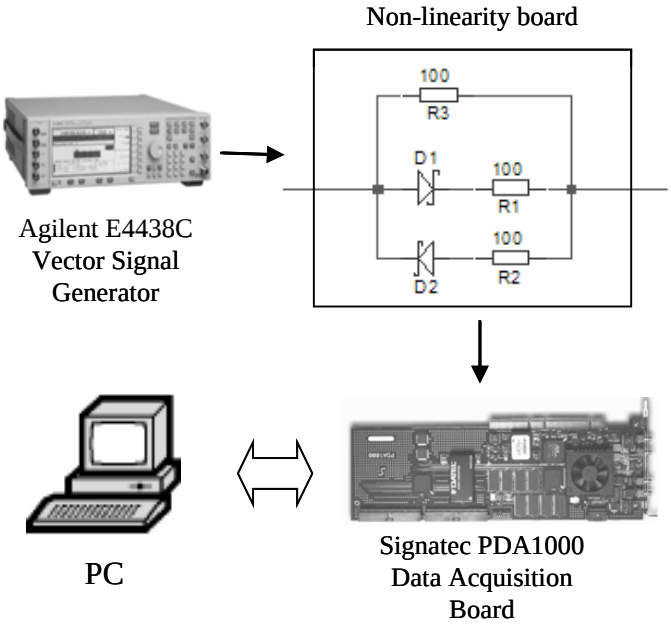

Figure 5. Test setup for the correction method.

Then, a second phase of tests has been carried out using W-CDMA signals compliant to the 3GPP standard [11]. Signals coming from a single Dedicated Physical Channel have been generated at a 15 MHz IF and acquired with a 250 MS/s sampling frequency. In Fig. 7 the PSD of the signal before correction is reported in grey colour, while for the PSD of the signal after the correction is shown in black. The graphs are reported in dB referred to the higher harmonic component. How it can be seen, the effect of the non-linearity is well compensated and the SFDR is increased from 14.88 dB to 36.08 dB.

V. Conclusions

The experimental validation of a method for digital compensation of high frequency, low resolution ADC non-linearity errors has been presented. In particular the compensation method has been validated on 3rd generation mobile telecommunication signals, compliant to 3GPP specifications and a SFDR increase of more than 20 dB has been achieved both on simulated and on actual W-CDMA signals. Further work is directed to experimental investigations using different telecommunication signals and to the integration of this method with some specific measurement method for 3G systems.

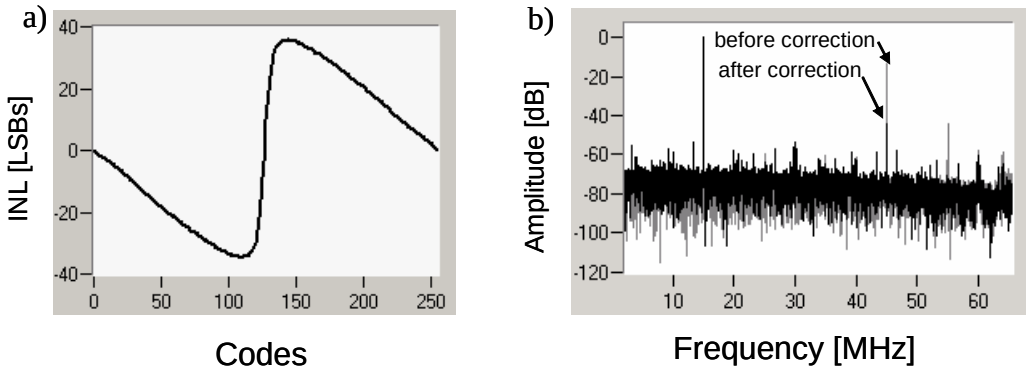

Figure 6. (a) INL introduced by the non-linearity board, and (b) the results of the correction method for a sinusoidal test signal.

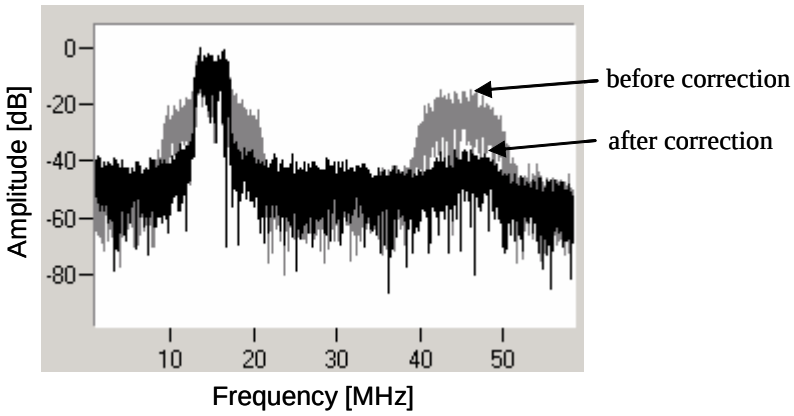

Figure 7. Power spectral density of a W-CDMA signal before and after the correction.

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