Digital to Analog Converters: a Metrological Overview

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Abstract- In the last years the technology improvement of Digital-to-Analog Converters (DACs) has extended the use of digital techniques in a multitude of applications. Consequently, there is an increasing attention to DAC topics, from researchers and manufacturers. The paper is aimed at providing a metrological overview and the leading trends of the research in the field of DACs.

I. Introduction

Digital computing power has exponentially increased at ever smaller incremental costs. With this powerful abundance, many applications formerly performed with analogue circuitry have found a new lease-on-life in this digital realm. Hot application areas include compact disc players, telecommunications, computer sound cards, digital instrumentation, computer graphic adapters [1].
However, the real world still is and will always be an analog place. To bring digital processing and its benefits on real-world applications, the analog signal must be translated into a format that a digital computer can utilize. This is the function of the Analog-to-Digital Converter (ADC). After processing by a digital computer or Digital Signal Processor (DSP), the resulting digital stream of information must be returned to its analogue form by a Digital-to-Analog Converter (DAC). Analog once again, the information can be "consumed" by the human senses, most often sight or hearing.
As a consequence, it is clear that the ADCs and the DACs are the bottleneck from the analogue world to the digital one, and vice versa, respectively. Therefore, particular attention has to be paid to these components both from the design point of view and from the metrological characterisation point of view. Papers, conferences, standards are mainly oriented to the analysis of the ADCs, less investigated it seems the metrological characterization of the DACs.
These components are crucial in emerging applications such as telecommunications, where the DAC puts the information on the line and a wide frequency band and high resolution are needed to meet the requirements on high speed and high accuracy. For these reasons, DACs are receiving an increasing attention, as testified by the growing amount of scientific contribution in this field. Moreover, the Waveform Measurement and Analysis Technical Committee (TC-10) of the IEEE Instrumentation and Measurement Society is working on a new project to produce a DAC standard [2]. This paper is aimed at providing a metrological overview of DAC topics by referring to: i) DAC architectures and technology trends, ii) DAC modelling, iii) DAC testing, and iv) DAC standardization.

II. DAC Architectures and technology trends

This section focuses on the new developments and the leading trends of high performance DACs. Concerning high speed DACs the current-steering architecture is the most discussed while for high accuracy DACs the oversampling DAC architecture is usually preferred.
For the majority of communication circuits, the most commonly used high-speed DAC is the current-steering architecture. Typically, an N-bit current steering DAC is designed using a segmented architecture in which input bits are divided into two groups with B less significant bits switching binary coded current sources and (N-B) most significant bits switching thermometer coded unary current sources. A layout dependent switching sequence that minimizes the systematic errors is presented in [3]. Using the results in [4] as a basis, a new cost-oriented approach to optimize the design area is developed. The optimum design can be obtained by reducing the area of the current source transistors. The designed DAC has a small size in comparison to equivalent subsystems reported in the literature.

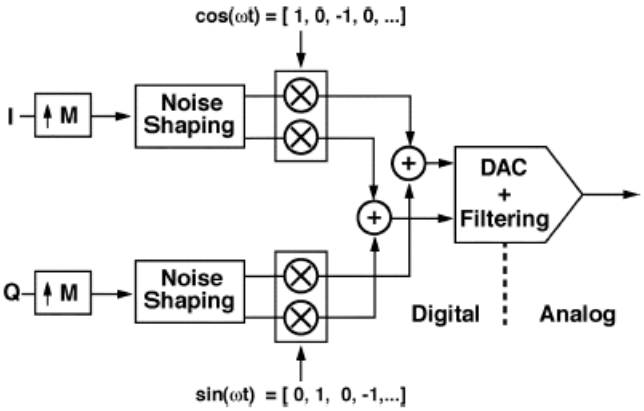

Figure 1. DAC architecture proposed in [7].

A 12-bit 320-MSample/s current-steering D/A converter in 0.18-μm CMOS is presented in [5]. In order to achieve high linearity and Spurious Free Dynamic Range (SFDR), a large degree of segmentation has been used, with the seven most significant bits (MSBs) being implemented as equally weighted current sources. A "design-for-layout" approach has allowed this to be done in an area of just 0.44 mm^2. The increased switching noise associated with a high degree of segmentation has been reduced by a new latch architecture.

Stability analysis of high-order Σ-Δ loops is a challenge. In [6] stable high-order error-feedback Σ-Δ DACs were designed based on a sufficient stability criterion. This analytical criterion claims that an error-feedback modulator with L^{th}-order FIR noise transfer function and L+1 bits is stable. Such error-feedback DACs are robust and achieve better performance than output-feedback architectures. Due to aggressive noise shaping and multibit truncation, simulations show that these DACs can achieve high resolution even for low oversampling ratios.

An oversampling bandpass DAC has been designed in [7] to eliminate the carrier leak and in-band SNR degradation that accompany I and Q channel mismatch in wireless transmitters. The converter combines a cascaded noise-shaping Σ-Δ modulator with digital FIR and mixed-signal semi-digital filters that attenuate out-of-band quantization noise (Fig. 1). The performance of the converter in the presence of current source mismatch has been improved through the use of bandpass data weighted averaging.

A photonic implementation of DAC is proposed in [8] using electrooptic polymer modulators. There are many advantages of using photonic technology to implement D/A conversion, such as high-speed clocking and sampling, wide-bandwidth, lightweight components, and reduced interference. A 2-bit implementation at low frequencies is experimentally demonstrated at a conversion rate of 80 MS/s which is limited by the bandwidth of the photodetector and its associated electronics.

Today, 24-bit resolution accompanied by excellent performance from a single low-cost miniature package is standard. CMOS technology reigns in areas where density must accompany low power and low supply voltages. BiCMOS takes precedence where speed and resolution must be combined with superior ac and dc performance. Progress in process technologies is letting designers pack multiple high-performance, high-resolution DACs on one die. In addition, more functions and features are being integrated without compromising performance, while keeping the power budget under control and the cost attractive. Driven by some emerging applications, integration is on the rise. Both precision analog and fast digital circuits can reside side by side on a single System on Chip (SoC) solution using the lowest-cost, highest-density standard CMOS process available from any foundry. The Δ-Σ architecture continues to dominate high-resolution DACs that run at slow to moderate speeds. As they exploit the state-of-the-art CMOS technology, these converters permit more functionality on-chip. They also allow multiple such units to be integrated on the same die for multiple-channel applications. Hybrid solutions will continue to take advantage of the fastest and greatest DAC chips on the market, combining them with the necessary functions and peripherals for a given application. In that way, they will deliver a complete high-performance solution from a single module [9].

III. DAC Modelling

The rapid diffusion of emerging high-performance standards for communication, measurement and entertainment purposes requires DACs with higher speed and accuracy so their design and testing become more challenging [10]. For this reason, DAC modelling research is almost always oriented to help designers to obtain converters having the best performance in terms of speed and accuracy.

Two DAC modelling techniques based on principles of wavelet theory are described in [11]. Macro modelling that uses passive components and adders and mathematical equations to depict the wavelet basis functions are proposed. To model the behaviour of DAC using wavelet theory, basis functions should be identified first. To do this, the output signal of the DAC is analysed in the time and in the

frequency domain. The proposed basic block diagram for DAC modelling consists of: i) a glitch generator, ii) a damped sine wave generator, iii) an exponential function generator, and iv) an adder.

Concerning current-steering DAC, several papers have proposed various models of the Integral NonLinearity (INL) as a function of the variance of the current source mismatch. However, most of these methods neither describe accurately the statistical behaviour of the INL and Differential NonLinearity (DNL) nor do they take into account the effects of the segmentation on the INL and DNL. In [12] it has been demonstrated that the segmentation of the current sources affects the statistical behaviour of the INL and DNL. Moreover, regression models for the DNL and INL are presented providing to evaluate the matching requirements of the current source of the current steering DAC as a function of segmentation ratio. It has been also demonstrated that with more than two segmented bits, the INL is the limiting factor.

For current-steering DACs, the delay difference among the current sources is one of the most important nonlinearity errors. In [13] a mathematical model that explains the impact of delay differences on the Spurious Free Dynamic Range (SFDR) of a thermometric DAC is proposed. This theoretical analysis shows that the delay differences among the current sources limit the DAC SFDR even when the signal frequency is very low. According to this result it is suggested to the designers to reduce the delay differences or find out some optimized delay distribution in order to improve DAC performance.

In the past, dynamic element matching techniques were presented to tackle static mismatch of current-steering DACs. However, little attention was directed to dynamic errors problems. In [14] several implementations to tackle with dynamic errors while avoiding performance degradation due to static error sources are presented. Dynamic errors in current-steering DACs are analysed through a dynamic error model to show that they contribute to nonlinearity in a different way as static mismatch errors.

The paper [15] is aimed at making easy the automation of the circuit design of future current-steering DACs. Two current source cell topologies, namely a simple cell and a cascoded cell (Fig. 2), are considered in [15] to obtain the relation of transistors design parameters to the static and dynamic models. On one hand, a mismatching statistical analysis is applied to all the transistors of the current source circuit. This allows the definition of design expressions relating the circuit parameters to the DAC specifications without the need of arbitrary design margins or Monte Carlo simulations. On the other hand, an improved analysis of the current source switching characteristics provides a more realistic modelling of the relation between transistors sizes and output current settling time. By including these two improved models into the usual design procedure, circuit sizing for optimum settling time and proper static behaviour can be obtained analytically, leading to smaller current source area, and, hence, to an overall DAC area reduction.

The effect of nonlinearities on DAC resolution is studied in [16]. Two models, an exponential and a sinusoidal approach, are proposed to estimate the drop in SIgnal to Noise And Distortion ratio (SINAD). These models were used to study the performance loss of a multi-bit DAC when used in frequency synthesizer architecture. From results obtained in [16], it follows that the amplitude errors should not be neglected for DACs that have less than 8-bit resolution as they degrade considerably the accuracy of the synthesizer output. However, using at least 8 bits implies larger die area and higher circuit complexity, as the use of compensation techniques might be required. Authors suggest the choice of a 1-bit Σ-Δ architecture for the DAC to be used in a synthesizer because its transfer function is inherently linear and the converter resolution can be adapted by changing operating frequency and a single voltage reference.

Segmented architectures are often used in DACs. A DAC structure based on recursive decomposition of an N-bit binary DAC in two (N-1)-bit DACs and one 1-bit DAC is proposed in [17]. A DAC model that includes matching errors has been simulated to develop optimal segmentation.

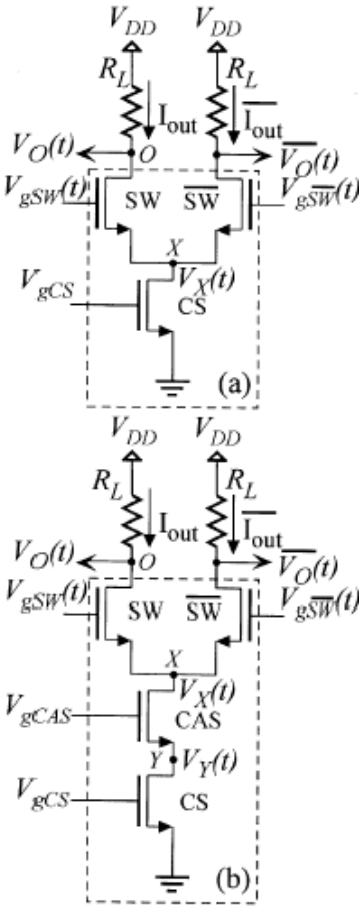

Figure 2. Current source cell topologies: (a) basic; (b) cascoded [15].

IV. DAC Testing

Due to the exponential growth in DAC internal complexity there is a major increment in testing time and equipment cost [18]. In order to reduce the total time necessary to carry out the static testing of a given N-bit DAC, parameters such as offset error, gain error, INL and DNL should be estimated by measuring the analog outputs corresponding only to a suitable subset of all possible 2^N input codes. This approach is increasingly convenient as the converter nominal resolution grows and it becomes particularly valuable when high volumes of production are considered. However, a reduction in the number of input test vectors requires the definition of appropriate mathematical models able of describing the influence of each elementary part of a given DAC architecture on its actual output voltages [19,20,21]. Once this data is known, the static testing efficiency can be improved by selecting only the input codes that enable the estimation of the most significant errors of the DAC. Interesting methods have been proposed to minimize the number of input codes aimed at testing both specific device families [22] and basic DAC schemes [23,24]. A more general approach is proposed and justified in [10]. This approach is based on a high-level model that takes advantage of the basic structural features common to most high-performance DACs (Fig. 3), thus enabling a major reduction in the total number of input test vectors. The efficiency improvement resulting from this procedure not only decreases the overall testing time, but it also promotes the design of both inexpensive Built-In Self-Test (BIST) architectures and digital self-calibration schemes.

BIST is a part of any complex SoC design. The DAC is one of the most commonly used mixed signal block in a SoC. It requires both static and dynamic tests [25]. BIST schemes for testing static parameters, including the gain and offset errors, DNL and INL, follow three approaches. In the first approach, suggested in [26], tests are performed to check if any of the errors exceed the ±0.5 LSB bounds. This scheme uses multiple voltage references and a precision gain amplifier. In an attempt to reduce the number of required reference voltages, in [27] a variable gain amplifier is introduced to amplify different codes to the same level and then compare it with a single reference. The second approach is to use the DAC in a feedback loop. In the scheme proposed in [28], the input to the DAC in the feedback path of a Σ-Δ modulator is switched between two codes with opposite signs. Static errors are inferred from the average value of the output, measured using an up/down counter. In [29] a scheme is proposed whereby the output of the DAC used in a successive approximation ADC is to be first sampled. This is converted back to a digital code by reconfiguring the system as an ADC. The difference between the two codes is a measure of the static errors in the DAC. In the third approach, a high frequency clock is used and static parameters are measured in terms of the number of clock cycles. In the scheme proposed in [30], the time taken by a linear ramp to cross the two consecutive levels is considered as a measure of corresponding step. In [31] the DAC output voltage to control a VCO and obtain errors in terms of the frequency shift is used. Accurate on-chip voltage or current references are difficult to get. A relatively more accurate time reference can be obtained from an external crystal oscillator. This is the solution adopted in [31]. However, they require a VCO with linearity better than that of DAC over the entire output range. This is difficult to achieve.

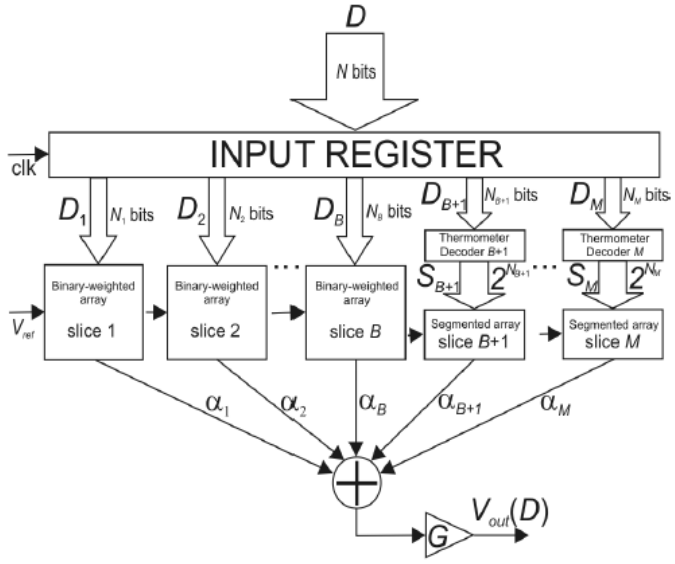

Figure 3. General block diagram showing the structure of high accuracy DACs based on the combination of binary-weighted and thermometer-encoded sections [10].

In [32], a modification of the scheme, which reduces the linearity requirements of the VCO is proposed. The tests are based on estimating the voltage step corresponding to adjacent codes. This is done using an on-chip offset-compensated sample and subtract module and a VCO. An up-down counter is used to measure the frequency and the reference clock is used to generate the counting window. The differential DAC output is connected to the sample and subtract module through switches. Computation of DNL is made from the estimated step size. Then, the computation of INL is made from DNL.

V. DAC Standardization

Due to their numerous features and wide range of application uses, it is very difficult to define a unique way in which DACs can be specified and tested. For this reason it is growing the need for DAC standardization. At the present time the existing main DAC standards are: (i) IEEE Std. 749 which addresses the testing of Analog-to-Digital and Digital-to-Analog converters, used for PCM television video signal processing [33], (ii) JEDEC Standard 99, addendum number 1, which deals with the terms and definitions used to describe Analog-to-Digital and Digital-to-Analog converters and does not include test methods [34], and (iii) EBU Technical Information I15-1998 [35] which reports ADC and DAC performance parameters for testing in conformity with ITU-R Recommendations BT.601 and BT.656. However, it does not exist a standard focusing specifically on terms, definitions and test methods for DACs for a wide range of applications as already done for ADCs (IEEE Std. 1241 [36]). In order to fill this lack the Waveform Measurement and Analysis Technical Committee (TC-10) of the IEEE Instrumentation and Measurement Society is working to realize a standard to provide common terminology and test methods for the testing and evaluation of DACs. The information in this standard will be useful both to manufacturers and users of DACs because it will provide a basis for evaluating and comparing existing devices, as well as providing a template for writing specifications for the procurement of new ones. Moreover, in some applications, the information provided by the tests described in this new standard could be used to correct DAC errors.

VI. Conclusions

DAC topics are becoming a very attractive research field as testified by the increasing amount of scientific contributions. In the paper a metrological overview of DAC has been presented. The paper can help young researchers interested in DACs to orientate themselves in this research field. Due to the rising amount of activities in this field and the quickness with which they evolve in the time, the Authors beg readers pardon in advance for all the omission surely present in this paper, mainly due to time, space and manpower limits.

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