A new approach to linearity and intermodulation errors estimation in digital to analogue converters

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Abstract – Static testing and diagnostics of digital to analogue converters involve the measurement of the nonlinearity of the converter and the successive estimation of suitable error terms, namely linearity and intermodulation errors. At the state of art, the estimation of the aforementioned error terms is performed by means of two linear transformations, which are applied to the nonlinearity array characterizing the converter. The computational burden of this approach could be too heavy; moreover, practical relations for assessing the uncertainty affecting the results are not available.

An alternative approach for estimating linearity and intermodulation errors is studied and proposed in this paper. By exploiting some nice features of the bit error functions, very straightforward relations that facilitate the estimation of the error parameters and allow a direct evaluation of the uncertainty affecting the results are defined. A number of laboratory tests on an actual D/A converter are conducted in order to assess the reliability and efficiency of the proposed approach.

I. Introduction

The static nonlinearity of digital-to-analogue (D/A) converters can be represented by means of the error terms, namely linearity and intermodulation errors, and error response. The interest in linearity and intermodulation errors arises from their capability of highlighting defects in the hardware of the converter, which makes them a useful diagnostic tool at disposal of technicians involved in production and testing.

The estimation of linearity and intermodulation errors from the measured nonlinearity requires the inverse error response of the converter. It has been proved [1]-[3] that the inverse error response can be represented by two linear transformations, namely ***W***, which is the Walsh transformation, and ***T***, which is a specific linear transformation that extracts the error terms from the Walsh spectra of the nonlinearity. Both ***W*** and ***T*** transformation are represented by means of matrixes whose size enlarges exponentially upon the increasing of the number of bits of the converter. As a consequence, if careful attention is not paid to the management of the available memory resources, the calculation of the inverse model could show itself heavy and time-consuming, especially in the presence of high-resolution converters. Moreover, the transformation described by ***T*** makes the evaluation of the uncertainty characterizing the estimates almost unpractical.

Therefore, an alternative approach for estimating linearity and intermodulation errors is studied and presented in this paper. In particular, it is shown that the error terms can be organized into different groups in order to separate the original problem into a sequence of smaller problems that are solved through a small number of very straightforward relations with a consequent and direct benefit on the uncertainty evaluation.

A brief overview concerning linearity and intermodulation errors affecting D/A converters and their role in the adopted model of such converters is first given. The proposed approach is then presented in detail, with references to a clarifying example; it is, in particular, emphasized that the same results attained by applying ***W*** and ***T*** transformation are gained applying very straightforward relations, which, in addition, allow practical evaluation of the uncertainty characterizing the error terms estimates. Finally, the results of nonlinearity measurements and error terms estimations carried out on an actual D/A converter are shown.

II. D/A converter model

An ideal unipolar *N-bit* D/A converter shows a perfectly linear relationship between the input code, a decimal integer, *m*, which is represented by a sequence of binary digits $d^m_1 d^m_2 \ldots d^m_N$, and the output voltage. It can be analytically described by:

$$V_n(m) = V_R \cdot \sum_{i=1}^{N} \frac{d_i^m}{2^i} \qquad m = 0 \ldots 2^N\text{-}1 \quad ; \qquad (1)$$

where V_R is the DC reference voltage, and $V_n(m)$ the nominal voltage for code *m*.
In an actual converter systematic errors cause differences between the actual output, V_{out}, and the ideal one. These differences define an array ***u*** whose values are dependent on the input code *m*:

$$\boldsymbol{u}(m) = \boldsymbol{V_{out}}(m) - V_R \sum_{i=1}^{N} \frac{d_i^m}{2^i} \qquad m = 0\ldots 2^N\text{-}1 \quad . \qquad (2)$$

These errors are caused by structural defects, precisely, by erroneous weights of the individual bits. Therefore, suitable correction terms, ε_i, referred to as linearity errors, should be applied to the ideal weights in order to attain a more reliable model of the actual converter:

$$\boldsymbol{V}_{out}(m) = V_R \cdot \sum_{i=1}^{N} d_i^m \left(\frac{1}{2^i} + \varepsilon_i \right) \qquad m = 0\ldots 2^N\text{-}1 \quad . \qquad (3)$$

Unfortunately, the superposition of linearity errors is not sufficient to describe all systematic errors that $\boldsymbol{u}$ accounts for. This is due to unavoidable effects, which are inherent to the functioning of the converter itself. The actual weight of individual bits, in fact, may depend on the state of all the other bits. These effects are addressed to interactions between bits, and are described by further correction terms, ε_{ij}, ε_{ijk},… $\varepsilon_{1\ldots N}$, called intermodulation errors. There are intermodulation errors due to the interaction of *2* or more bits up to *N*. The number of interacting bits is referred to as order of intermodulation. Therefore, the output voltage of an actual D/A converter is described by:

$$\boldsymbol{V}_{out}(m) = V_R \left(\sum_{i=1}^{N} \frac{d_i^m}{2^i} + \varepsilon_0 + \sum_{i=1}^{N} d_i^m \varepsilon_i + \sum_{i=1}^{N} \sum_{j=i+1}^{N} d_i^m d_j^m \varepsilon_{ij} + \sum_{i=1}^{N} \sum_{j=i+1}^{N} \sum_{k=j+1}^{N} d_i^m d_j^m d_k^m \varepsilon_{ijk} + \ldots + d_1^m d_2^m \ldots d_N^m \varepsilon_{12\ldots N} \right)$$
$$m = 0\ldots 2^N\text{-}1 \quad . \qquad (4)$$

the error term ε_0 is named zero-order intermodulation error.

The difference of the real and ideal output characteristics of the converter, which is the nonlinearity $\boldsymbol{u}$, can be expressed by a linear combination of suitable basic arrays each of them multiplied by a corresponding error term. The basic arrays and corresponding error terms are distinguished by the same subscripts:

$$\boldsymbol{u} = V_R \left(\varepsilon_0 \, \boldsymbol{ef_0} + \sum_{i=1}^{N} \varepsilon_i \, \boldsymbol{ef_i} + \sum_{i=1}^{N} \sum_{j=i+1}^{N} \varepsilon_{ij} \, \boldsymbol{ef_{ij}} + \sum_{i=1}^{N} \sum_{j=i+1}^{N} \sum_{k=j+1}^{N} \varepsilon_{ijk} \, \boldsymbol{ef_{ijk}} + \ldots + \varepsilon_{12\ldots N} \, \boldsymbol{ef_{12\ldots N}} \right) \quad . \qquad (5)$$

Each array highlights the effects of the corresponding error term on the nonlinearity exhibited by the D/A converter. These basic arrays represent the bit error functions. They are defined for each value of the input code and can assume only the value *1* or *0*. In particular, for the input code *m*, their value is *1* only if the corresponding error term gives a contribution to $\boldsymbol{u}(m)$. For instance, the zero order intermodulation error ε_0 affects all voltage values, thus, the corresponding array, $\boldsymbol{ef_0}$, is one for each value of *m*. The linearity error ε_i, instead, affects all voltage values produced by input codes with the i^{th} bit switched-on; its contribution is taken into account by the array $\boldsymbol{ef_i}$, which is *1* if bit d_i is switched-on and *0* otherwise. In the same way, the m^{th} coefficient of the array $\boldsymbol{ef_{ij}}$, which describes the interaction of bits *i* and *j*, assumes the value *1* if both bits in the binary representation of code *m* are switched-on, otherwise the value *0*. These arrays are easily attained taking the product of the arrays associated to the individual interacting bits: in other terms, $\boldsymbol{ef_{ij}}$, is the element by element multiplication of $\boldsymbol{ef_i}$ and $\boldsymbol{ef_j}$.

The nonlinearity $\boldsymbol{u}$ can be represented in compact form by means of matrix $\boldsymbol{A}$, and array $\boldsymbol{\varepsilon}$ that records all error terms. The columns of matrix $\boldsymbol{A}$ are the arrays representing the bit error functions. The error terms are typically arranged in order to have first the zero order intermodulation error, then the linearity errors, then the second order errors up to the N^{th} order intermodulation term. As an example the error response of a 3 bit converter is given by:

$$\boldsymbol{u} = V_R \, \boldsymbol{A}\,\boldsymbol{\varepsilon} = \begin{pmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 1 & 1 & 0 & 0 & 1 & 0 \\ 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 0 & 1 & 0 & 1 & 0 & 0 \\ 1 & 1 & 1 & 0 & 1 & 0 & 0 & 0 \\ 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \end{pmatrix} \begin{pmatrix} \varepsilon_0 \\ \varepsilon_1 \\ \varepsilon_2 \\ \varepsilon_3 \\ \varepsilon_{12} \\ \varepsilon_{13} \\ \varepsilon_{23} \\ \varepsilon_{123} \end{pmatrix} \quad . \qquad (6)$$

III. Proposed approach

In order to estimate the error terms the inverse error response is needed. Determining the inverse model can be an heavy and time consuming task, especially in the presence of high-resolution D/A converters, due to the large size of matrix $\boldsymbol{A}$. Anyway, if the problem is properly approached, the estimation of the linearity and intermodulation errors can be straightforwardly carried out. In particular, the original problem is separated into a set of *N+1* problems, being *N* the number of bits of the converter, which can be solved by means of simple relations. In the following subsections, the theoretical framework of the proposed approach is presented; the problem of evaluating the uncertainty characterizing the estimates is faced; finally an application example is shown.

A. Theoretical framework

The proposed approach exploits some nice features characterising the bit error functions. For the sake of clarity the description is aided by Fig.1 and Fig.2, that show, for a 3 bit converter, the bit error functions associated respectively to the zero order intermodulation and linearity errors (Fig.1), and those associated to the second and third order errors (Fig.2).

Initially, the normalization of the nonlinearity $\boldsymbol{u}$ to the reference DC voltage V_R is required:

$$\boldsymbol{u_R} = \boldsymbol{u} / V_R \quad . \qquad (7)$$

Then the estimation of the zero order intermodulation error, ε_0, which is a constant error contribution to all elements in the normalized nonlinearity $\boldsymbol{u}$, is carried out. Being zero the value of all bit error functions except $\boldsymbol{ef_0}$ for $m=0$, and ε_0 the weight assigned to $\boldsymbol{ef_0}$, it is:

$$\varepsilon_0 = \boldsymbol{u_R}(0) \quad . \qquad (8)$$

The constant error contribution ε_0 is then subtracted from $\boldsymbol{u_R}$ in order to attain a new array $\boldsymbol{u_1}$ in which only linearity and higher order intermodulation errors, from the second up to the N^{th}, are present:

$$\boldsymbol{u}_1 = \boldsymbol{u}_R - \varepsilon_0 \, \boldsymbol{ef}_0 \quad . \qquad (9)$$

For the estimation of the linearity errors, the proposed approach relies on the property that any non-zero value recognized in $\boldsymbol{u_1}(2^{N-i})$ can be accounted only by the error function $\boldsymbol{ef_i}$, which is the unique bit error function, except $\boldsymbol{ef_0}$, that has non-zero value for code $m=2^{N-i}$:

$$\varepsilon_i = \boldsymbol{u}_1(2^{N-i}) \qquad i=1\ldots N. \qquad (10)$$

Concerning the estimation of the second-order intermodulation errors, the subtraction of the contribution of linearity errors from $\boldsymbol{u_1}$ is first required in order to attain $\boldsymbol{u_2}$:

$$\boldsymbol{u}_2(m) = \boldsymbol{u}_1(m) - \sum_{i=1}^{N} \varepsilon_i \, \boldsymbol{ef}_i(m) \qquad m=1\ldots 2^N. \qquad (11)$$

As a general rule, the estimation of higher-order intermodulation errors can be achieved only if lower order errors are known. Attained $\boldsymbol{u_2}$, it should be noted that a non zero value detected in $\boldsymbol{u_2}(2^{N-i}+2^{N-j})$ can be accounted only by function $\boldsymbol{ef_{ij}}$, which is the unique bit error function that exhibits non-zero value for $m=2^{N-i}+2^{N-j}$, except $\boldsymbol{ef_0}$, and $\boldsymbol{ef_i}$, $i = 1\ldots N$, whose contribution has been previously subtracted:

$$\varepsilon_{ij} = \boldsymbol{u}_2(2^{N-i} + 2^{N-j}) \qquad i=1\ldots N; \qquad j=i+1\ldots N. \qquad (12)$$

Henceforward, the relations for the estimation of higher order intermodulation errors can be easily derived. The last intermodulation error, i.e. the N^{th} order error, in particular is given by:

$$\varepsilon_{12..N} = \boldsymbol{u}_N\left(2^{N-1} + 2^{N-2} + \ldots + 2 + 1\right) \quad . \qquad (13)$$

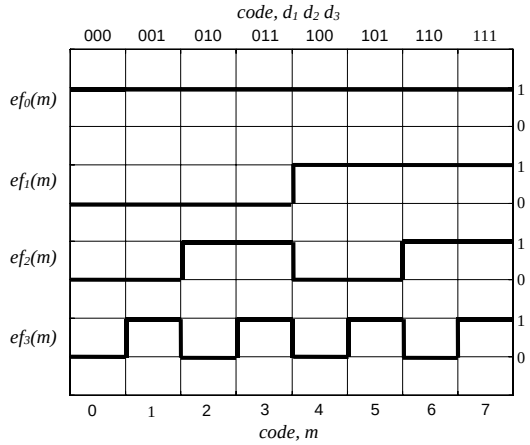

Fig. 1. Bit error functions associated to the zero-order intermodulation error and linearity errors for a 3-bit converter. The binary representation of the input code is given on the top horizontal axis; the decimal representation of the input code on the bottom.

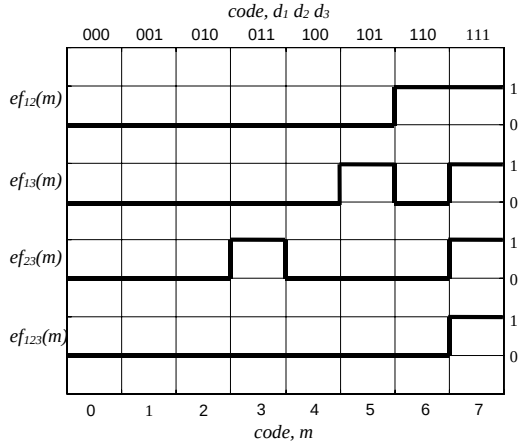

Fig. 2. Bit error functions associated to the intermodulation errors for a 3-bit converter. The binary representation of the input code is given on the top; the decimal representation of the input code on the bottom.

B. Uncertainty evaluation

The uncertainty characterizing DC voltage measurements typically depends on instruments' reading and range; as a consequence, each element $\boldsymbol{u_R}(m)$, $m = 0,\ldots,2^N-1$, of the normalized nonlinearity has to be characterized by its own standard uncertainty $\boldsymbol{\sigma_u}(m)$, $m = 0,\ldots,2^N-1$.

Each error term is represented by a linear combination of the elements of the normalized nonlinearity $\boldsymbol{u_R}$; precisely:

$$\boldsymbol{\varepsilon} = \boldsymbol{A}^{-1}\boldsymbol{u}_R \quad , \qquad (14)$$

where the matrix $\boldsymbol{A^{-1}}$ represents the inverse error response of the converter. Moreover, it can be easily shown [5] that the generic element b_{ij} of the i^{th} row, j^{th} column of matrix $\boldsymbol{A^{-1}}$, which is given by:

$$b_{ij} = \frac{(-1)^{i+j}\, Det(\boldsymbol{A}_{ij})}{Det(\boldsymbol{A})} \quad , \qquad (15)$$

in which *Det*( ) is the determinant operator and $\boldsymbol{A}_{ij}$ is the matrix attained from $\boldsymbol{A}$ by deleting the i^{th} row and j^{th} column, can be either *0*, or *1*, or *-1*. Therefore, each error term is given by a linear combination of some elements of the normalized nonlinearity $\boldsymbol{u_R}$, which are selected by the coefficients *+1* and *-1*.

Being the elements of $\boldsymbol{u_R}$ the results of independent measurements, the squared uncertainty characterising the estimate of error terms is expressed by the combination of uncertainty contributions by quadratic summation. In this case, uncertainty contributions must be just added, because the sensitivity coefficients are unitary. To this aim, the array $\boldsymbol{\sigma_u^2}$, which contains the squared uncertainty data, is processed in the same way as $\boldsymbol{u_R}$. In detail, $\boldsymbol{\sigma_u^2}$ is first assigned to $\boldsymbol{\sigma_u^2}_{0}$, which is the array at the initial step, then at the generic step, an updated version, $\boldsymbol{\sigma_u^2}_{k+1}$, is accomplished from $\boldsymbol{\sigma_u^2}_{k}$, adding by means of the error functions the specific uncertainty contribution due to the selected elements:

$$\begin{aligned}
&\boldsymbol{\sigma}^2_{u\,0} = \boldsymbol{\sigma}^2_u \\
&\boldsymbol{\sigma}^2_{u\,1} = \boldsymbol{\sigma}^2_{u\,0} + \boldsymbol{\sigma}^2_u(0)\,\boldsymbol{ef}_0 \\
&\boldsymbol{\sigma}^2_{u\,2} = \boldsymbol{\sigma}^2_{u\,1} + \sum_{i=1}^{N} \boldsymbol{\sigma}^2_u\left(2^{N-i}\right)\boldsymbol{ef}_i \\
&\boldsymbol{\sigma}^2_{u\,3} = \boldsymbol{\sigma}^2_{u\,2} + \sum_{i=1}^{N}\sum_{j=i+1}^{N} \boldsymbol{\sigma}^2_u\left(2^{N-i} + 2^{N-j}\right)\boldsymbol{ef}_{ij} \\
&\ldots
\end{aligned} \quad . \qquad (16)$$

The uncertainty related to the generic error of order *k*, whose value is recognized in $\boldsymbol{u_k}(m)$, is given by $\boldsymbol{\sigma_{u\,k}}(m)$. It is worth noting that the higher the order of the error term to be estimated, the higher the uncertainty characterizing the estimate.

C. Application example

To clarify the operative stages of the proposed approach a simulated case study is presented. In particular, a non-ideal 3-bit converter is considered; the differences between the ideal and actual output voltage and their uncertainty are given in Table I, which also shows the values of the error terms with their uncertainty.

TABLE I.
Differences between the ideal and actual output voltage and error terms with their uncertainty. The uncertainty characterizing the DC reference voltage, V_R, is assumed to be negligible.

Code		Normalized ideal output voltage	Normalized real output voltage (simulated)	$\boldsymbol{u_R} \pm \boldsymbol{\sigma_u}$	$\boldsymbol{\varepsilon} \pm \boldsymbol{\sigma_\varepsilon}$
m	$d_1d_2d_3$				
0	*000*	*0.000*	*0.000*	*0.000 ± 0.003*	$\varepsilon_0 = 0.000 \pm 0.0030$
1	*001*	*0.125*	*0.115*	*-0.010 ± 0.003*	$\varepsilon_1 = 0.040 \pm 0.0036$
2	*010*	*0.250*	*0.265*	*0.015 ± 0.003*	$\varepsilon_2 = 0.015 \pm 0.0042$
3	*011*	*0.375*	*0.365*	*-0.010 ± 0.002*	$\varepsilon_3 = -0.010 \pm 0.0042$
4	*100*	*0.500*	*0.540*	*0.040 ± 0.002*	$\varepsilon_{12} = -0.050 \pm 0.0048$
5	*101*	*0.625*	*0.685*	*0.060 ± 0.002*	$\varepsilon_{13} = 0.030 \pm 0.0051$
6	*110*	*0.750*	*0.755*	*0.005 ± 0.001*	$\varepsilon_{23} = -0.015 \pm 0.0056$
7	*111*	*0.875*	*0.855*	*-0.020 ± 0.001*	$\varepsilon_{123} = -0.030 \pm 0.0064$

$$\boldsymbol{u}_R = [0 \quad -0.010 \quad 0.015 \quad -0.010 \quad 0.040 \quad 0.060 \quad 0.005 \quad -0.020] \quad ; \qquad (17)$$

$$\boldsymbol{\sigma}^2_{u\,0} = \boldsymbol{\sigma}^2_u = [0.9 \quad 0.9 \quad 0.9 \quad 0.4 \quad 0.4 \quad 0.4 \quad 0.1 \quad 0.1] \times 10^{-5} \quad ; \qquad (18)$$

$$\varepsilon_0 = \boldsymbol{u_R}(0) \pm \boldsymbol{\sigma}_{u\,0}(0) = 0.000 \pm 0.0030 \quad ; \qquad (19)$$

$$\boldsymbol{u}_1 = \boldsymbol{u}_R - \varepsilon_0\, \boldsymbol{ef}_0 = [0 \quad -0.010 \quad 0.015 \quad -0.010 \quad 0.040 \quad 0.060 \quad 0.005 \quad -0.020] \quad ; \qquad (20)$$

$$\boldsymbol{\sigma}^2_{u\,1} = \boldsymbol{\sigma}^2_{u\,0} + \boldsymbol{\sigma}^2_u(0)\,\boldsymbol{ef}_0 = [1.8 \quad 1.8 \quad 1.8 \quad 1.3 \quad 1.3 \quad 1.3 \quad 1.0 \quad 1.0] \times 10^{-5} \quad . \qquad (21)$$

The evaluation of linearity errors produces the results:

$$\varepsilon_1 = \boldsymbol{u}_1(4) \pm \boldsymbol{\sigma}_{u\,1}(4) = 0.040 \pm 0.0036; \quad \varepsilon_2 = \boldsymbol{u}_1(2) \pm \boldsymbol{\sigma}_{u\,1}(2) = 0.015 \pm 0.0042;$$
$$\varepsilon_3 = \boldsymbol{u}_1(1) \pm \boldsymbol{\sigma}_{u\,1}(1) = -0.010 \pm 0.0042; \quad . \qquad (22)$$

The subtraction of linearity errors from $\boldsymbol{u}_1$ is then required:

$$\sum_{i=1}^{N} \varepsilon_i \, \boldsymbol{ef}_i = [0 \quad -0.010 \quad 0.015 \quad 0.005 \quad 0.040 \quad 0.030 \quad 0.055 \quad 0.045] \quad ; \qquad (23)$$

$$\boldsymbol{u}_2 = \boldsymbol{u}_1 - \sum_{i=1}^{N} \varepsilon_i \, \boldsymbol{ef}_i = [0 \quad 0 \quad 0 \quad -0.015 \quad 0 \quad 0.030 \quad -0.050 \quad -0.065] \quad ; \qquad (24)$$

$$\boldsymbol{\sigma}_{u\,2}^2 = \boldsymbol{\sigma}_{u\,1}^2 + \sum_{i=1}^{N} \boldsymbol{\sigma}_u^2 \left(2^{N-i}\right) \boldsymbol{ef}_i = [1.8 \quad 2.7 \quad 2.7 \quad 3.1 \quad 1.7 \quad 2.6 \quad 2.3 \quad 3.2] \times 10^{-5} \quad . \qquad (25)$$

The second order intermodulation errors are estimated as:

$$\varepsilon_{12} = \boldsymbol{u}_2(6) \pm \boldsymbol{\sigma}_{u\,2}(6) = -0.050 \pm 0.0048; \quad \varepsilon_{13} = \boldsymbol{u}_2(5) \pm \boldsymbol{\sigma}_{u\,2}(5) = 0.030 \pm 0.0051;$$
$$\varepsilon_{23} = \boldsymbol{u}_2(3) \pm \boldsymbol{\sigma}_{u\,2}(3) = -0.015 \pm 0.0056; \quad . \qquad (26)$$

The contribution of the second order intermodulation errors is then subtracted from $\boldsymbol{u}_2$ in order to evidence higher order errors:

$$\sum_{i=1}^{N} \sum_{j=i+1}^{N} \varepsilon_{ij} \, \boldsymbol{ef}_{ij} = [0 \quad 0 \quad 0 \quad -0.015 \quad 0 \quad 0.030 \quad -0.050 \quad -0.035] \quad ; \qquad (27)$$

$$\boldsymbol{u}_3 = \boldsymbol{u}_2 - \sum_{i=1}^{N} \sum_{j=i+1}^{N} \varepsilon_{ij} \, \boldsymbol{ef}_{ij} = [0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad -0.030] \quad ; \qquad (28)$$

$$\boldsymbol{\sigma}_{u\,3}^2 = \boldsymbol{\sigma}_{u\,2}^2 + \sum_{i=1}^{N} \sum_{j=i+1}^{N} \boldsymbol{\sigma}_u^2 \left(2^{N-i} + 2^{N-j}\right) \boldsymbol{ef}_{ij} = [1.8 \quad 2.7 \quad 2.7 \quad 3.5 \quad 1.7 \quad 3.0 \quad 2.4 \quad 4.1] \times 10^{-5} \quad . \qquad (29)$$

Finally, the third order intermodulation error is attained from array $\boldsymbol{u}_3$:

$$\varepsilon_{123} = \boldsymbol{u}_3(7) \pm \boldsymbol{\sigma}_{u\,3}(7) = -0.030 \pm 0.0064 \quad . \qquad (30)$$

IV. Experiments on an actual D/A converter

The experiments are carried out on an actual D/A converter characterized by 12 bits nominal resolution. In detail, they are executed by means of an automatic test equipment, which includes the converter under test, a digital multimeter, an external auxiliary source, and a control and processing unit, all interconnected by a standard IEEE-488 interface. The automatic test equipment is roughly sketched in Fig.3.

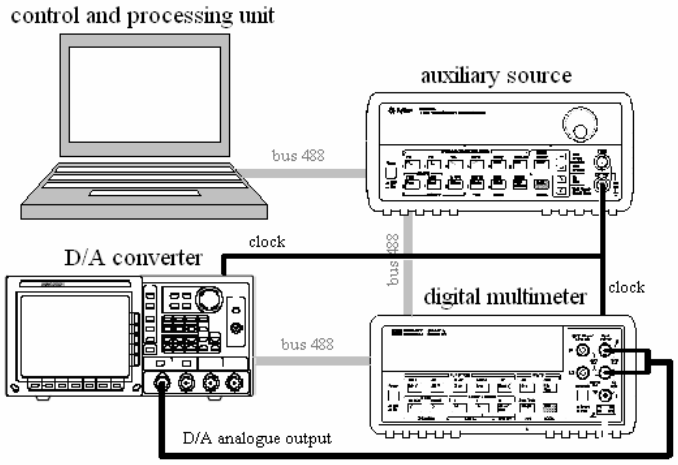

Fig.3 Automatic test equipment adopted for the experiments.

The external source provides a 10 Hz square wave that is applied as external clock to the D/A converter. The clock signal is contemporaneously used to trigger the digital multimeter that measures the analogue output levels produced by the D/A converter. In particular the D/A converter switches on the rising edge of the clock signal, while the multimeter is triggered on the falling edge. The 50 ms delay between the rising and the falling edges avoids errors that the dynamic effects due to switching in the D/A converter can introduce in static testing. The dynamic effects are characterized by a finite settling time, as it is shown in Fig. 4, where the output D/A level, the 10 Hz square wave clock signal and the VM-COMP signal provided by the multimeter are displayed. The VM-COMP signal is the low-true pulse offered by the multimeter after the completion of each DC measurement. In order to attain fast measurements and reduce time consumption, 5½ digits resolution is imposed, which is equivalent to about 17 bits resolution, and the LCD of the multimeter is disabled in the remote use.

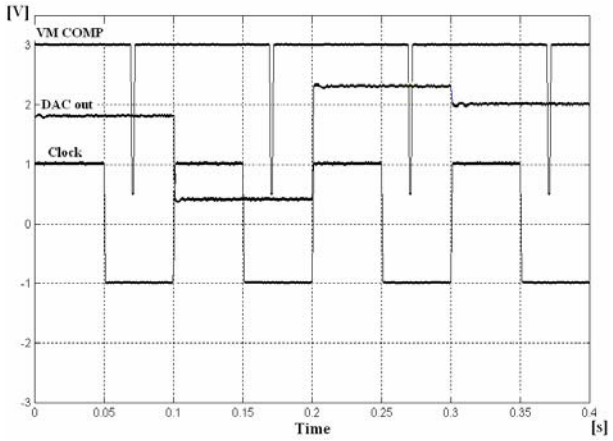

Fig.4 D/A level, 10 Hz clock and VM-COMP signal.

Processing nonlinearity data should verify, first of all, the absence of hysteretic effects in the D/A converter, otherwise the considered error response, which refers to linearity and intermodulation errors, is not appropriate. To this aim, the actual static transfer characteristic has been measured exciting randomly all the input codes, and the measurements have been repeated for different random excitations. The compatibility of the measurement results attained in the same environmental conditions has shown the absence of hysteretic effects.

Then, the difference between the static transfer characteristic of the converter under test and the nominal one has been calculated and passed to the data processing unit that implements the proposed approach for the evaluation of error terms. As an example Fig.5 shows the graphic of the linearity and intermodulation errors of the converter under test. The errors are sorted in order to have first the zero-order intermodulation error, then the linearity errors, then the second order up to the 12^{th} order intermodulation error. The error terms are enumerated from *0* up to 2^N*-1*. The most relevant errors are the linearity and lower order intermodulation errors, which are shown in Fig.5 b), a portion of Fig.5 a).

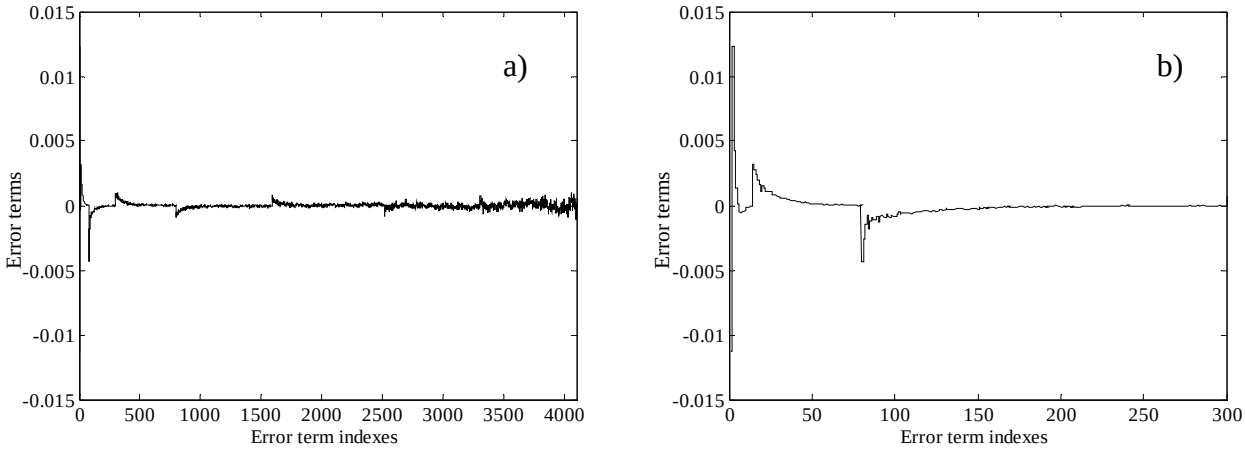

Fig. 5 Graphics of linearity and intermodulation errors. Error terms are enumerated from the zero order intermodulation term up to the N^{th} order terms. Linearity errors follow the zero order term and proceed the second order term in the enumeration. In particular, b) is a portion of a) highlighting the values of linearity, second order and third order intermodulation errors.

V. Conclusions

A new approach for estimating linearity and intermodulation errors affecting digital to analogue converters has been presented. It exploits some nice features of the bit error functions, which allow a very straightforward estimation of the error terms. In particular, the proposed approach grants the same results offered by alternative methods already presented in literature, with the further possibility of a straightforward evaluation of the uncertainty affecting the estimates. The results attained in laboratory tests have assessed the reliability and efficacy of the proposed approach. The ongoing research is focused on the investigation and analysis of alternative models to represent static errors affecting D/A converters.

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