Performances And Limitations Of A Technique For Background Calibration Of Capacitor Mismatch Errors In Pipelined A/D Converters

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***Abstract*-**This paper analyses the performances of a recently proposed background calibration technique with digital cancellation of D/A converter noise, which has been recently proposed for high-speed, high-resolution, pipelined Analog-to-Digital Converters (ADCs).

I. Introduction

The operation of pipelined A/D converters is mainly affected by the non-linearity of the A/D and D/A subconverters and by the interstage gain errors. A/D errors can be effectively eliminated by digital correction [1], provided that non-linearity does not exceed one half LSB.

Background calibration of DAC and interstage gain errors can be accomplished by one of the techniques recently reported in the literature [2]-[5]. A pseudo-random perturbation is introduced in the DAC operation, and the residue, quantized by the ADCs of the following stages, is correlated with the perturbation so as to identify and correct the effects of non-ideal weighting. Different architectures for the introduction of the random perturbation are at the heart of the various techniques. Among them, [4,5] address the calibration of gain and capacitor mismatch errors in a capacitive DAC-subtractor, directly driven by the thermometer code output of a flash ADC stage.

This paper first shows that, for a given resolution of the complete A/D converter, there is an upper bound to the mismatch error which can be corrected according to [4,5]. A novel procedure is provided for the correction of the residue, which, unlike [5], does not require neglecting second order error terms. Estimation of the mismatch parameters is then discussed. Finally, simulation results are provided to demonstrate the convergence of the mismatch parameter estimation and the performance improvement which can be achieved in a 14 bit converter with calibration of the first DAC.

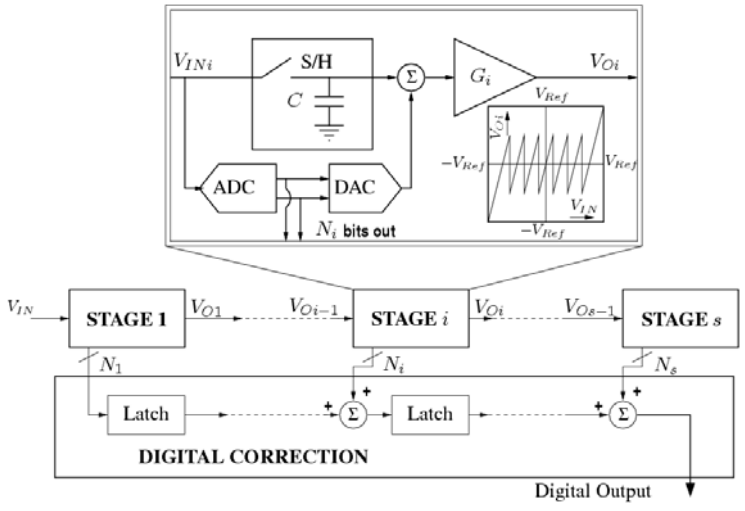

Figure 1. Pipeline ADC block diagram.

II. Calibration revisited

The considered pipeline architecture is shown in Fig.1. Each stage consists of a sample-and-hold amplifier (SHA), a low-resolution flash ADC with $2^{Ni} - 2$ comparators, a DAC, a subtractor and a residue amplifier. Also shown in the figure is the residue provided to the following stages as a function of the input signal. The switched capacitor multiplying DAC (MDAC) of Fig.2 plays the role of SHA,

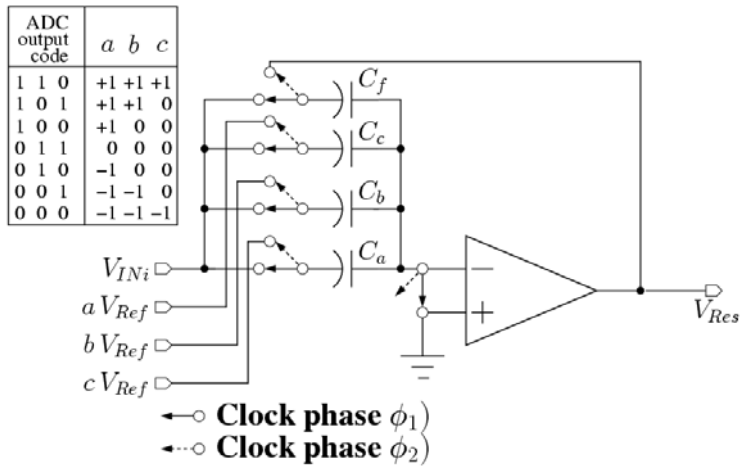

Figure 2. Simplified model of a 3-bit MDAC. During clock phase ϕ_2, capacitors C_a, C_b and C_c are connected, respectively, to $a\ V_{Ref}$, $b\ V_{Ref}$, and $c\ V_{Ref}$.

DAC, subtractor and residue amplifier at the same time. Control signals *a*, *b*, and *c* are provided by the flash ADC. Hereafter, reference will be made to the 3-bit MDAC reported in the figure, but the discussion can be easily generalized to any N_i-bit MDAC. The stage input voltage V_{INi} is sampled by the coarse sub-ADC and the MDAC at the same clock phase ϕ_1. In this phase all the G =4 identical capacitors of the MDAC are connected to V_{INi}, and the inverting input of the amplifier is shorted to ground, so that the charge at the input of the amplifier is $Q=V_{INi}\ C_{TOT}$, where $C_{TOT} = C_a + C_b + C_c + C_f$. In a second phase ϕ_2, the switch between the amplifier's inputs is opened, capacitor C_f is placed in the op-amp's feedback loop while the other capacitors are connected to ground or to $\pm\ V_{Ref}$ depending on the ADC output, coded by *a, b*, and *c* [5], thus determining the output voltage. Representing each capacitance C_a, C_b, … as $C_i = C_{TOT}\ (1 + \varepsilon_i) / G$, where C_{TOT} / G is the average of the four capacitances and ε_i is the i^{th} relative error, so that $\varepsilon_a + \varepsilon_b + \varepsilon_c + \varepsilon_f = 0$, and neglecting the finite op-amp gain and settling time, the output residue becomes

$$V_{\mathrm{Re}s} = \frac{C_{TOT}}{C_f} V_{INi} - \frac{aC_a + bC_b + cC_c}{C_f} V_{\mathrm{Re}f} = \frac{G}{1+\varepsilon_f} V_{INi} - \frac{\sum_{i=a,b,c} i(1+\varepsilon_i)}{1+\varepsilon_f} V_{\mathrm{Re}f} \qquad (1)$$

Notice that $G=4$ is the nominal gain of the MDAC. Since $V_{INi}/V_{Ref} = (a+b+c)/G + E$, where E is the quantisation error of the flash ADC, the normalised residue, $\hat{V}_{\mathrm{Re}s} = V_{\mathrm{Re}s} / V_{\mathrm{Re}f}$, becomes

$$\hat{V}_{\mathrm{Re}s} = \frac{G}{1+\varepsilon_f} E - \frac{a\varepsilon_a + b\varepsilon_b + c\varepsilon_c}{1+\varepsilon_f} \qquad (2)$$

The difference $\delta = \hat{V}_{\mathrm{Re}s} - GE$ represents the error arising from capacitor mismatch.

The calibration procedure requires shuffling, at each sampling instant, the four capacitors according of the scheme of Table 1 [5]. P_1, P_2, and P_3 are zero-mean, pseudo-random binary variables with values ±1 which define how the four physical capacitors C_1, C_2, C_3, and C_4 are assigned to the role of C_a, C_b, C_c, and C_f.

Table 1 – Shuffling scheme.

P_1	P_2	P_3	C_a	C_b	C_c	C_f
-1	-1	-1	C_3	C_2	C_4	C_1
-1	-1	+1	C_4	C_2	C_3	C_1
-1	+1	-1	C_3	C_1	C_4	C_2
-1	+1	+1	C_4	C_1	C_3	C_2
+1	-1	-1	C_1	C_4	C_2	C_3
+1	-1	+1	C_1	C_3	C_2	C_4
+1	+1	-1	C_2	C_4	C_1	C_3
+1	+1	+1	C_2	C_3	C_1	C_4

Shuffling alone only reduces the non-linearity of the converter at the expense of an increase of time-varying noise δ. However, with some algebrical manipulation, it may be shown that, without any approximation,

$$a\varepsilon_a + b\varepsilon_b + c\varepsilon_c = -\frac{1}{G}\left[\sum_{i=1}^{3} P_i\Delta_i\gamma_i + P_1P_2\Delta_2\gamma_{12} - P_1P_3\Delta_3\gamma_{12}\right] \tag{3}$$

$$\varepsilon_f = -\left(\sum_{i=1}^{3} P_i\Delta_i - P_1P_2\Delta_2 + P_1P_3\Delta_3\right) \tag{4}$$

where $\Delta_1=\varepsilon_1+\varepsilon_2-\varepsilon_3-\varepsilon_4$, $\Delta_2=\varepsilon_1-\varepsilon_2$, $\Delta_3=\varepsilon_3-\varepsilon_4$, $\gamma_1=-a+b-c$, $\gamma_2=\gamma_3=a-b-c$, and $\gamma_{12}=a+b-c$.

It is apparent that by substituting (3) and (4) in (2) it is possible to determine the correct value at each sampling instant if Δ_1, Δ_2, and Δ_3 are known. Note that, unlike in [5], if the Δ_i are known without error, the exact value of the residue *GE* can be determined using (2), since no second order error terms are neglected.

However, in order to obtain an estimate of the mismatch parameters Δ_i , it is necessary to linearise (2), so that δ is approximated by

$$\hat{\delta} = -\left(a\varepsilon_a + b\varepsilon_b + c\varepsilon_c + GE\varepsilon_f\right) \tag{5}$$

On these grounds, following the theory proposed in [5] with minor deviations, mismatch parameters Δ_i can be estimated as

$$\tilde{\Delta}_i = G\frac{\mathsf{E}\left\{P_i\hat{V}_{Res}\gamma_i\right\}}{\mathsf{E}\left\{\gamma_i^2\right\}+\mathsf{E}\left\{\gamma_i\hat{V}_{\mathrm{Re}s}\right\}} \tag{6}$$

where $\mathsf{E}\{\cdot\}$ represents the expectation operator, and the assumption is made that $\mathsf{E}\{\gamma_i\, GE\}\approx\mathsf{E}\{\gamma_i\,\hat{V}_{\mathrm{Re}s}\}$.

Since non-linearity is a major concern in high-resolution converters, it is convenient to consider the errors arising from the linear approximation underlying (5). The amplified residue is known with the finite resolution n_b of the following stages. Fig.3 reports, as a function of n_b, the maximum error observed in the estimate $G\tilde{E}=\hat{V}_{\mathrm{Re}s}-\hat{\delta}$ proposed in [5] with respect to $GE=\hat{V}_{\mathrm{Re}s}-\delta$. Each point in the plot represents the average of the maxima observed over 20 simulations with Gaussian ε_i; 100 kSamples are considered in each simulation. When the resolution is low, the error converges as expected to one half LSB of the n_b bits of the following stages. For high resolution, the errors saturate to a value of the order of ε^2 because of the non-linear terms neglected in (5). Thus, if the approach suggested by [5] is followed, given the standard deviation of the errors ε_i in a specific stage, it is possible to roughly determine the maximum equivalent resolution n_b beyond which no improvement is possible. This limitation does not exist if (2), (3), and (4) are used for the correction as suggested in the present paper. However, it should be noted that it is necessary to resort to the linearised approximation (5) for the practical estimation of the Δ_i.

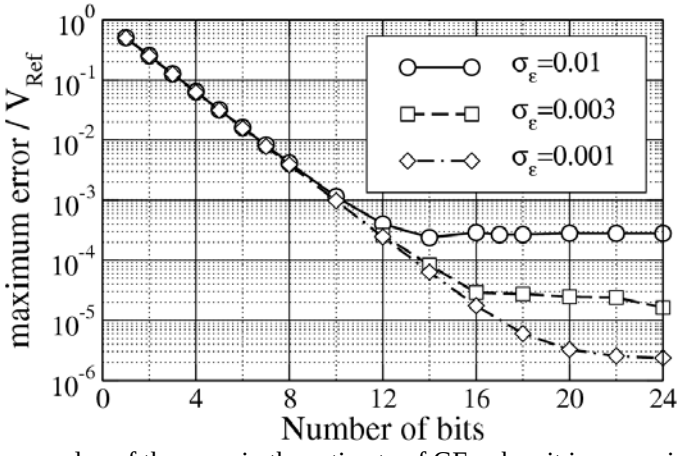

Figure 3. Maximum value of the error in the estimate of GE, when it is approximated as $\hat{V}_{\mathrm{Re}s}-\hat{\delta}$

III. Simulation results

Based on the above theory a Simulink-Matlab model of a background calibrated, pipelined A/D converter was developed. A first set of tests concerns the convergence of the estimation of mismatch parameters Δ_i using (6).

Fig.4 shows how the parameter $\tilde{\Delta}_1$ converges to the true value Δ_1: the lower lines represent the

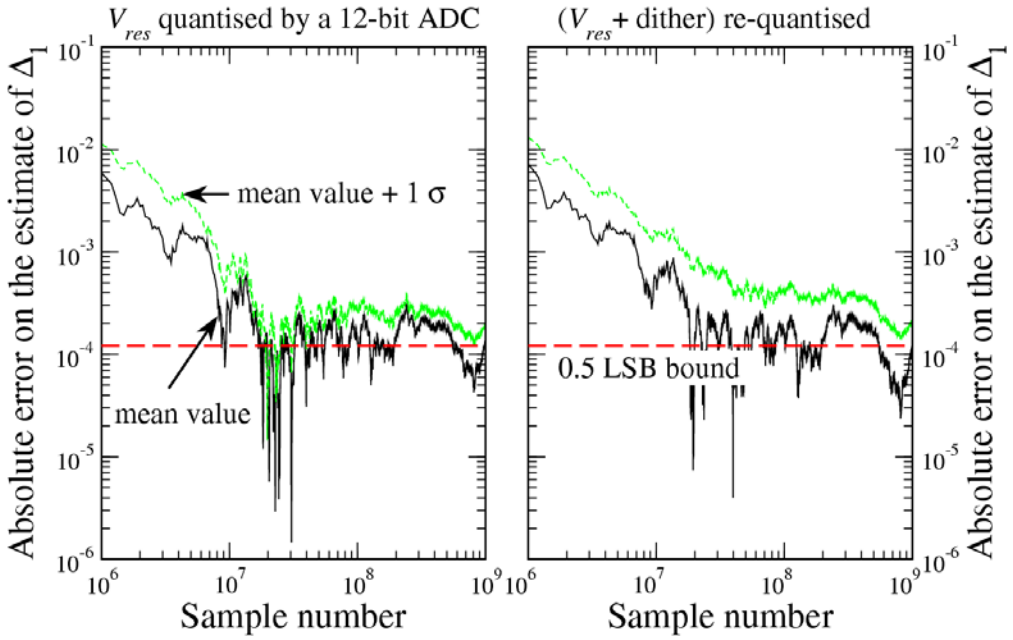

Figure 4. Error on the estimated value of Δ_1 as a function of the averaged number of samples. Left: the residue is quantised by a 12-bit converter. Right: the residue is re-quantised by a three-level quantiser.

absolute value of the average error $\left(\tilde{\Delta}_1 - \Delta_1\right)$ estimated over 20 simulations. The abscissa represents the number of samples used for the estimation of the expected value. The input signal was a 90% full-scale sinewave with offset, no overflow. The figure to the left corresponds to the case where $\tilde{V}_{Res}$ in (6) is quantised by a 12-bit converter representing the following stages; the figure to the right corresponds to the case where a uniform 11-bit dither is added to the quantised residue, and the result is re-quantised by a 3-level quantiser. As shown in [5], this allows a considerable hardware reduction. These results, like the others obtained for $\tilde{\Delta}_2$ and $\tilde{\Delta}_3$, seem to support that the errors tend to one half LSB of the quantiser used for estimating the residue. There is no substantial difference between the case where the residue is quantised by a 12-bit ADC and the case where dither is added and the dithered residue is processed by a three-level quantiser. The upper lines represent the same value plus one standard deviation estimated from the 20 simulations. It was found that the standard deviation converges to approximately $1/\sqrt{12}$ LSB in the case of 12-bit residue quantisation. While this result could be expected, the apparent stabilisation of the mean value around 0.5 LSB is rather surprising. In the case of dithering, the standard deviation seems to decrease more slowly and does not stabilize until 10^9 samples.

Based on this estimator of mismatch parameters Δ_i, a simplified model of a 14-bit A/D converter with background calibration of the first three bit stage was developed. Fig. 5 shows the effectiveness of the mismatch-noise cancellation procedure once the parameters Δ_i are estimated using 10^9 samples. The upper line represents the noise power observed when shuffling only is applied, without noise cancellation. Circles and squares correspond to the noise power observed when noise is cancelled using the Δ_i estimated by 12-bit quantisation of the residue and, respectively, when the Δ_i are estimated by dithering and 3-level re-quantisation. When 12-bit quantisation is used the noise power closely corresponds to
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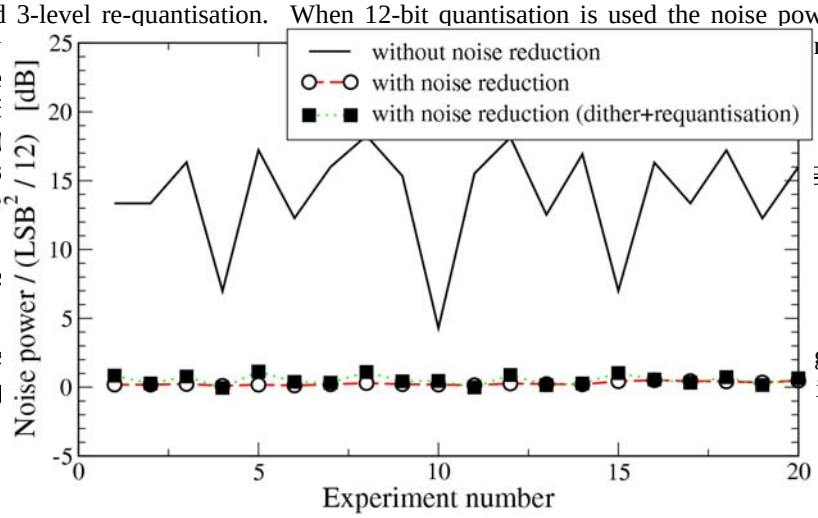

Figure 5. Noise power referred to the ideal quantisation noise.

that quantisation noise masks the error underlying the approximation in (8).

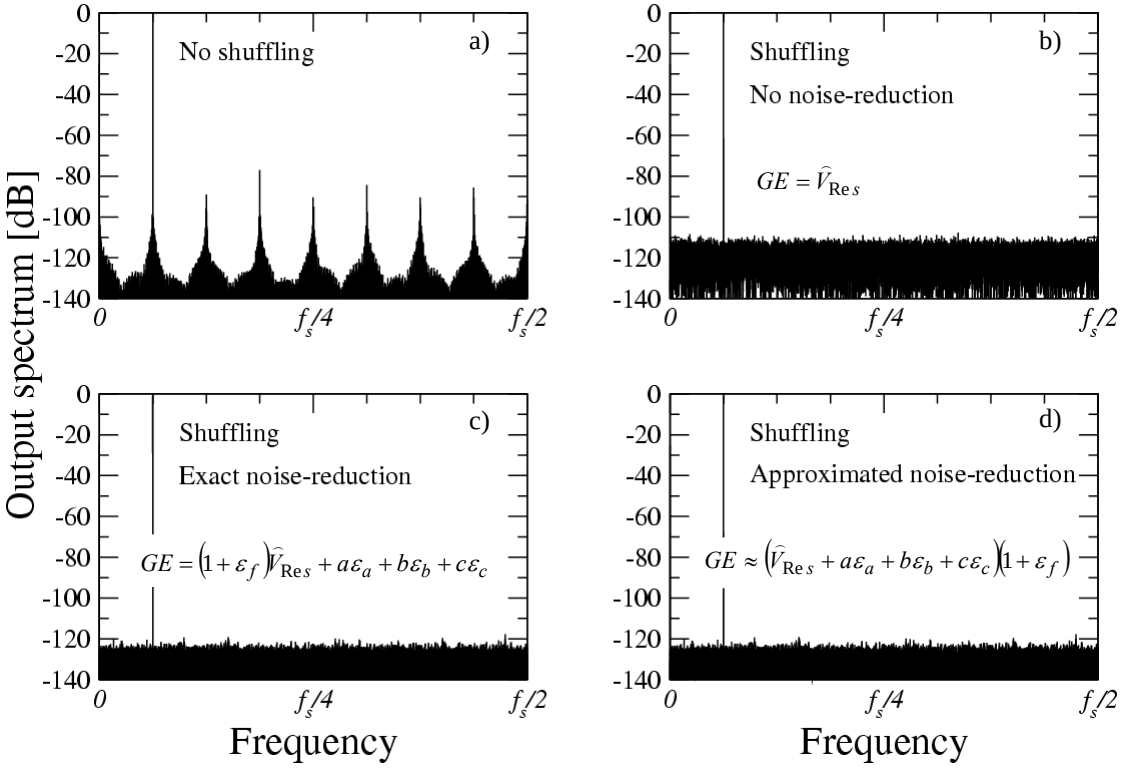

Figure 6. Output spectrum when a 14-bit A/D converter samples a sinewave. a) No shuffling, b) shuffling alone, c) and d) mismatch-noise cancellation.

IV. Conclusions

Mismatch-noise cancellation in pipelined A/D converters, according to the procedure described in [5], was evaluated. For a given mismatch level, a bound on the maximum resolution of the converter which is compatible with the use of the approximated correction formula suggested in [5] was provided, together with an exact correction procedure. Simulations show that mismatch parameters of the order of 10^{-3} in the first 3-bit stage of a 14-bit ADC can be estimated with an uncertainty of the order of the 12-bit resolution of the following stages after acquiring a number of samples of the order of 10^9. The overall performances of the technique seems satisfactory, even if hardware is simplified by resorting to dithering and 3-level re-quantisation of the first stage residue.

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