Dynamic Errors Of Integral Nonlinearity Measured By Histogram

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Abstract **–** The dynamically tested INL and its hysteresis was measured by the sine-wave histogram. The model of ADC with the hysteresis is tested by a simulation. The suitability of the hysteresis as a complemetary description to INL is discussed in the paper.

I. Introduction

The ADC (analog-to-digital converter) nonlinearity can be measured by the sine-wave histogram method. The result of the method is assumed meaningful in case when the ADC with only static nonlinearity is tested or when the ADC dynamic nonlinearity is negligible due to the low frequency of test signal. The histogram test presumes that ADC is monotonic and has no hysteresis [1]. Although the condition of the monotonic transfer curve is fulfilled at today's fast ADC, the transfer curve of this ADC has substantial hysteresis. Nevertheless, an attempt to measure the dynamic integral nonlinearity and the hysteresis of a fast, flash ADC was performed.

The ADC with dynamic nonlinearity can be described by the model depicted in Fig.1. It consists of the cascade of non-linear function f_1, f_2, the ideal sampler and the ideal quantization unit.

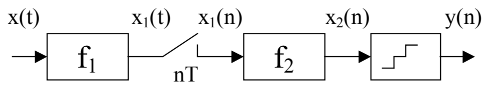


Figure 1. ADC model

For the Nyquist application of ADC or when nonlinear functions f_1, f_2 are static, i.e. memory-less, the distortion blocks can be united. However, for the undersampling application ADC with the dynamic nonlinearity it makes sense to use the f_2 block. The problem with missing f_2 block arises from the fact, that no link to previous sample $x_1(n-1)$ is feasible. On other hand, the missing f_1 block results in neglecting distortions related to the slew rate of input signal.

The histogram test based on analysis of two separate probability distributions, the first for rising values and the second for falling values of y(n), is mentioned and disputed in [2]. This is the case of missing f_1 block. Besides, the sorting samples to rising and falling ones with no previous knowledge of input signal frequency results in either the narrowing of usable code space for the calculation or in the necessity to largely overdrive the ADC. This makes this test not feasible for the input frequencies close to the odd multiplies of Nyquist frequency. Also the simple calculation of transition levels from the cumulative histogram is impossible due to the natural single-side cut-off of the separated probability distributions. The case with the missing block f_2 is common, e.g. in [3].

The dynamic nonlinearity of f_1 or f_2 can be described as two-valued function [2,3]:

$$f = g(x) + sign(s) \cdot h(x), \qquad (1)$$

where g(x) is static nonlinearity (average characteristic) and h(x) is the hysteresis (deviation from the average characteristic) and sign(s) is sign function of slew rate of x. The function g(x) is the origin of the in-phase harmonic distortion, while h(x) causes the out-of-phase harmonic distortion. More complex and accurate non-linear behaviour is described by the phase plane [3]:

$$f = g(x, s), \qquad (2)$$

where s is slew rate of signal x.

II. Hysteresis

The hysteresis is considered to be the non-linear behaviour with memory, signal direction dependent and slew-rate independent. Because the hysteresis represents dynamic non-linear distortion in the ADC and it is frequency- and amplitude-dependent, we use hysteresis only just as a simple description of more complex ADC nonlinearity. The common definition of a non-linear device with hysteretic input is [2]

$$y = g_x(x) \mp h_x(x), \qquad (3)$$

where x and y are input and output signals, g_x is the static nonlinearity and h_x is the hysteresis related to input.

The output signal is defined for the rising and falling input signal as y_1 and y_2, respectively

$$y_1 = g_x(x) - h_x(x)$$

$$y_2 = g_x(x) + h_x(x). \qquad (4)$$

Although this is the simple, natural, and common [2] definition, the inverse definition would be more useful for the histogram test of ADC

$$x = g_y(y) \pm h_y(y), \qquad (5)$$

with h_y the hysteresis related to output. With the assumption that g_x, g_y are monotonic functions, it is possible to construct the inverse function g_y to the function g_x so, that equation (3) and (5) are equivalent. However, this is not possible with the hysteresis function h_y. Two values of input signal x_1, x_2 are defined for the rising and falling output signal and for one value of output y

$$x_1 = g_y(y) + h_y(y)$$

$$x_2 = g_y(y) - h_y(y). \qquad (6)$$

The extension of (6) for the ADC results in equation with the output code k

$$x_1 + q_1 = T[k] + INL[k] + H_y[k] = f_1[k]$$

$$x_2 + q_2 = T[k] + INL[k] - H_y[k] = f_2[k], \qquad (7)$$

where q_1, q_2 are quantization errors, T[k] is the ideal k^{th} code transition level, INL[k] and $H_y[k]$ are the integral nonlinearity and the hysteresis. The offset error and the gain error are neglected. We assume that the transfer characteristics f_1, f_2 are monotonic vectors and thus the ADC has no missing codes for both the rising and the falling output signal. We also suppose that the signal is bellow the full-scale and so the histogram test and the complex spectrum test can be done together in one measurement. The transfer characteristics f_1, f_2 are equal at least at two points k_{min} and k_{max}, which represent the peaks of digitised signal. This is assured by the hysteresis

$$H_y[k_{min}] = H_y[k_{max}] = 0. \qquad (8)$$

The properties of two types of hysteresis H_x, H_y are demonstrated in a simple example with a triangle hysteresis (H_{max} = 0,3) in Figure 2. Obviously, the input-related hysteresis H_x generates only out-of-phase harmonics, including out-of-phase carrier. On the contrary, the output-related hysteresis H_y results in both the in-phase and the out-of-phase harmonics. However, with the sufficiently low hysteresis the out-of-phase harmonics dominates.

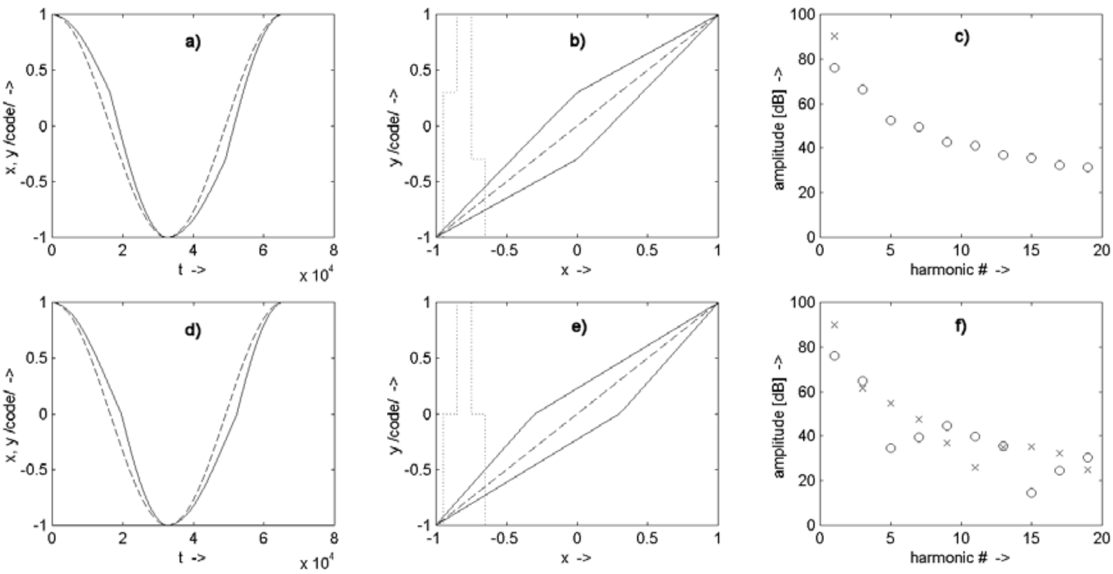


Figure 2. Input- (a,b,c) and output- (d,e,f) related hysteresis.
Time plot, x-y plot and spectrum, 'x' – real part, 'o' – imaginary part.

The histogram test of the integral nonlinearity INL[k] is based on collecting the code histogram D[k] of sine-wave signal. The calculation of INL[k] from the histogram is well described in [1], the cumulative histogram, the transition levels and the differential nonlinearity are computed at first. The hysteresis of integral nonlinearity can be computed in similar way. The samples are collected in two different histograms, one for the rising output samples D_1 and one for the falling output D_2.

The hysteresis is evaluated from the differential hysteresis DH_y similarly the integral nonlinearity from the differential nonlinearity:

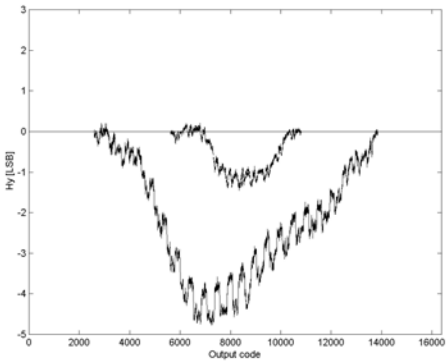
$$H_y[k] = \sum_{i=k_{\min}}^{k} DH_y[k] = \sum_{i=k_{\min}}^{k} \left(\frac{2 \cdot D_1[i]}{D_1[i] + D_2[i]} - 1 \right). \qquad (9)$$

In the Figure 2b,e, the schematic plot of the 'rising' and 'falling' normalised histograms is showed in the (x,y) plot. While the sum of the normalised histograms of the output related hysteresis is constant, the non-constant sum of histograms of the input-related hysteresis results in a non-zero integral nonlinearity. Hence, the output hysteresis H_y could be regarded as a suitable complementary description to the INL.

III. Measurements

To test the utility of hysteresis function to characterize ADC nonlinearity a set of measurements was done. The testing board developed at our institute with AD6644, 14-bit, 65 MHz ADC and 64K FIFO was used. All hysteresis histogram tests were performed for 25M samples, input signal of 90,031425 MHz and coherent sampling signal of 29,982720 MHz. Those values fulfil the condition of the uniform distribution of samples in phase from 0 to 2π [1]. The low alias frequency is suitable for hysteresis test, because hits of the codes in the histogram border are not limited considerably. The level of input signal was bellow full-scale, so the complex spectrum can be investigated in parallel. However, full width of histogram can not be used because of a weak AM modulation of the test signal and a small DC drift, the necessary restriction was about 2x20 LSB (-50 dBc).

In figure 3, the results of hysteresis from rising/falling histograms are shown for the full-scale signal and -6 dBFS signal. The dramatic change of hysteresis functions is visible when small (5 LSB rms) wide-band dither was added. In another measurement (not shown), the small change of input frequency (10^{-5}) resulted also in considerable change of hysteresis. In Figure 4, the measurement of INL on a half code interval was tested with -6dB signal. Although the shape of INL measured on half scale segment is similar to the INL measured on full-scale they differ in details considerably. As expected, the dynamically measured INL is changing considerably in all measurements with the small change of the signal frequency and amplitude and the condition of the measurement (e.g. additive noise). The dynamic errors of ADC are dominant and hardly predictable.



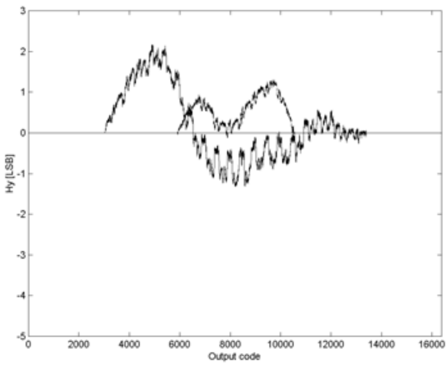


Figure 3. Hysteresis at full-scale signal and –6dB signal, no dither (left), with dither (right).

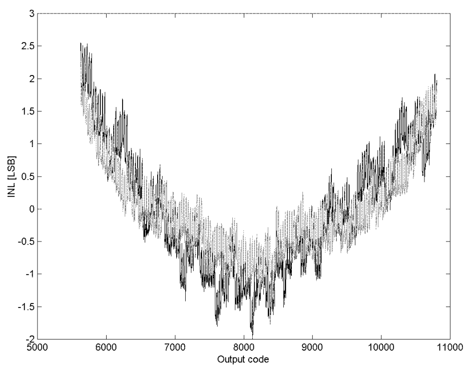


Figure 4. INL segment measured at full-scale and –6dB (gray line) signal, no dither.

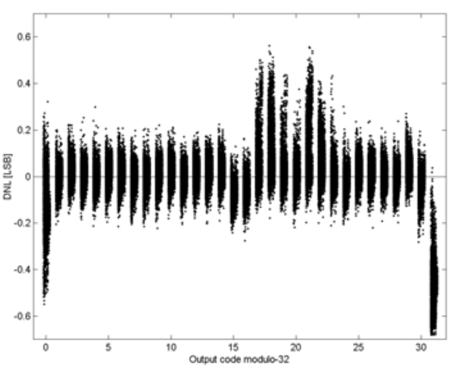


Figure 5. DNL modulo-32 plot for various sampling and input signals (F_S 30 and 60 MHz, F_{IN} 90.03 and 61.5 MHz

During the INL tests of the AD6644 ADC, also the behaviour of DNL was investigated over a wide range of combinations of the sampling frequency and the amplitude and frequency of input signal. The maximal and minimal DNL is changing slightly from 0.5 to 0.6 LSB and from –0.6 to –0.5 LSB, respectively. In Figure 5 is shown 32-modulo graph of DNL errors plotted over wide range of input and sampling signals. The different measurements are represented by a slight shift on code axis. The strong periodicity of DNL is linked to the nonlinearity of the last stage (5 bits valid) of AD6644 pipeline flash architecture (5-5-6 bits). It would be useful to use dither of 64 LSB peak-to-peak in order to randomise the repeated DNL errors [6].

IV. Simulation

The simulation of the ADC model with hysteresis defined by (7) was performed in order to check the validity of INL and hysteresis obtained from histogram of acquired data. The result is a comparison of the INL and hysteresis before and after the simulation. In addition, the complex spectrum of the simulated signal is compared with the spectrum of the actual signal (Fig. 6). The signal frequency of the simulated input signal is the same as of the actual signal. The amplitude is slightly lower (-0.03 dB) than of the actual signal, because the INL and hysteresis characteristics were limited necessarily as mentioned above. The data size was 12,5M samples, a uniformly distributed dither of 3 LSB peak-to-peak was added to the harmonic signal.

acquisition $\rightarrow$ *histogram* $\rightarrow$ *INL,* H_y $\rightarrow$ *ADC simulation* $\rightarrow$ *histogram* $\rightarrow$ *INL,* H_y
$\swarrow$ $\swarrow$
complex spectrum *complex spectrum*

Figure 6. Simulation chart

In Figure 7a, the INL and the hysteresis of acquired data are shown. The hysteresis is mirrored in the plot (dashed line) in order to distinguish it from the INL and to point out its functionality. Note that while a natural inertial hysteresis is expected to be positive, the measured hysteresis is negative. The INL and the hysteresis obtained from the simulation are in Fig. 7d. The histogram test outputs are also shown for the model with no hysteresis (Fig. 7b) and for the one with no INL (Fig. 7c). From the Figure 7, it can be concluded, that INL and hysteresis parameters are mostly independent and the INL is repeated exactly by the simulation. However, the hysteresis from the simulation differs from the original in details.

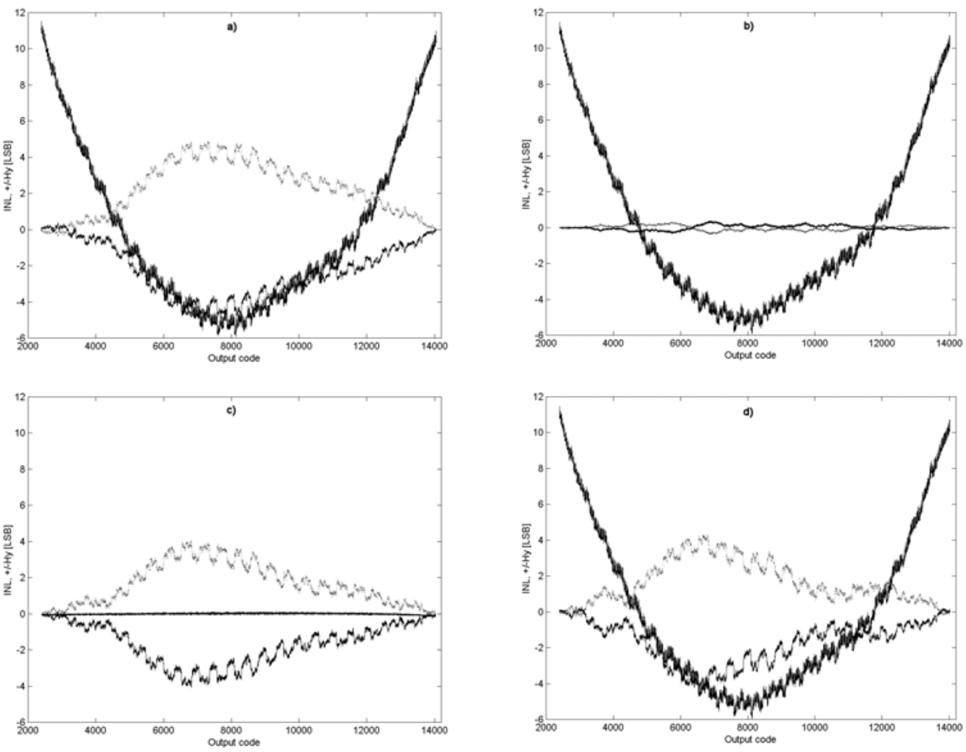


Figure 7. INL and hysteresis H_y of acquired data a), simulation with INL b), simulation with hysteresis c) and simulation with INL and hysteresis d).

The spectra of the acquired data and simulated data (with the same parameters as in Fig.7) are compared in Figure 8. The low order in-phase harmonics (2nd to 9th) of simulation and of actual signal are within 3 dB, the error of out-of-phase harmonics is up to 30 dB. However, the domination of out-of-phase harmonics (3rd, 6th, 9th) is preserved by the simulation. The difference of simulated and actual high order harmonics (Fig. 8b) is essential. Nevertheless, the origin of in-phase and out-of-phase distortion is visible (INL, hysteresis). In order to suppress the noise of the actual signal, many data blocks were used for harmonic evaluation. Each 64K sample was phased on the carrier after FFT, so the data blocks are summed coherently. The level of noise peaks of the simulated signal is depicted in the figure (dashed line).

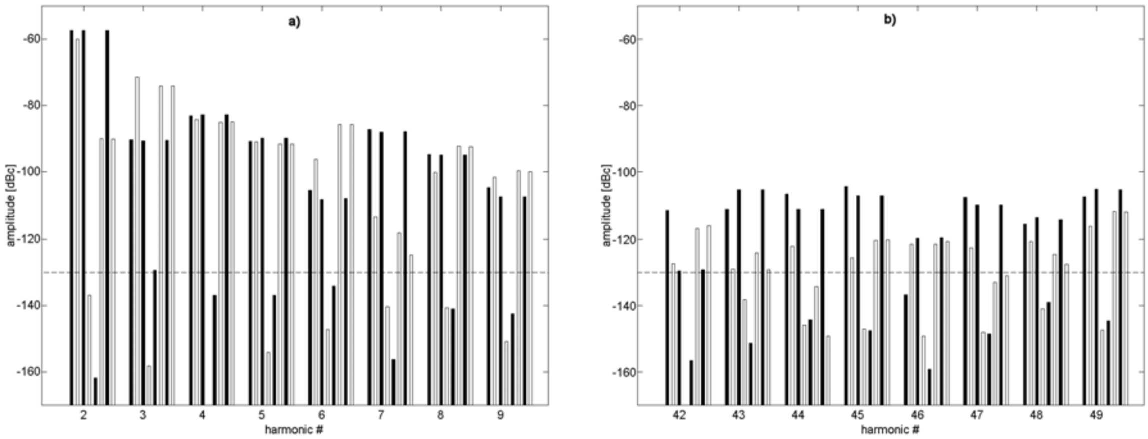


Figure 8. Low-order a) and high-order harmonics b) of (i) acquired signal, (ii) simulated signal with INL, (iii) simulated signal with hysteresis, (iv) simulated signal with INL and hysteresis (from left to right), in-phase harmonics – black bar, out-of-phase harmonics – white bar.

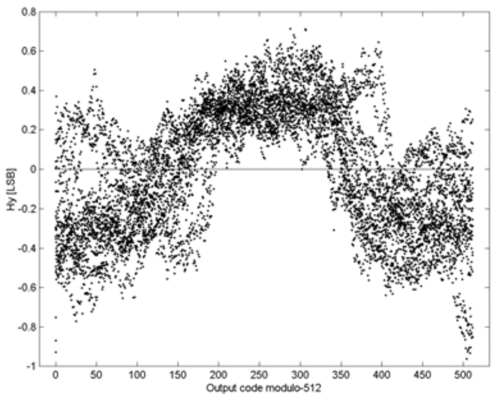


Figure 9. Hysteresis modulo-512 plot (mean value of segments forced to zero)

In Figure 7c, a strong periodicity of hysteresis is visible. The periodicity with the period of 512 is highlighted in Figure 9. The periodicity of hysteresis is linked to the nonlinearity of the middle stage (4 bits valid) of AD6644 pipeline flash architecture (5-5-6 bits). It would be useful to use a dither of 1024 LSB peak-to-peak in order to randomise these repeated errors.

The second simulation was done with simple triangle functions as the INL and the hysteresis parameters of the simulation (Figure 10a). The results (Figure 10b,c,d) are similar to the first simulation, the INL is reproduced perfectly, but the shape of hysteresis differs. Nevertheless, the INL and hysteresis seem to be independent parameters.

Finally, the signal, whose histogram test parameters are shown in Fig. 10c (pure hysteresis), is split into two signals by means of FFT and inverse FFT. The first part is the signal with in-phase harmonics only; the out-of-phase distortions are zeroed. The second part is the signal with out-of-phase harmonics, the in-phase harmonics unless the carrier and DC are zeroed. The INL and hysteresis of these signals are shown in Fig.11. It can be concluded that out-of-phase harmonics result in strong hysteresis and a minor INL (Fig.11a), which seems to be mutually annulled at the complete signal (Fig.10c) by the INL from in-phase harmonics (Fig.11b). The description of interactions between the signal parameters (the in-phase and out-of-phase harmonics) and the histogram test outputs - ADC distortion parameters (the INL and the hysteresis) are demonstrated in Figure 12. This behaviour is in accordance with the impact of out-of-phase distortion to the INL mentioned in [5].

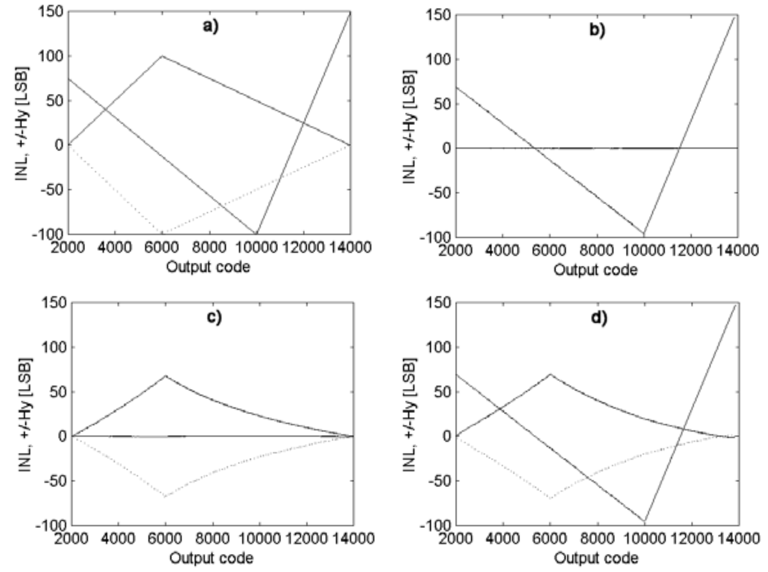


Figure 10. Enforced INL and hysteresis H_y a), simulation with INL b), simulation with hysteresis c), simulation with INL and hysteresis d).

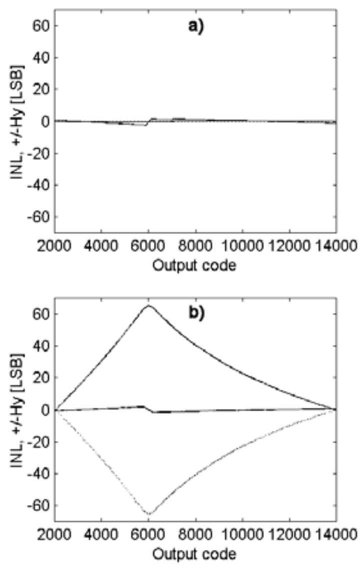


Figure 11. INL and hysteresis of signal from Fig. 10c, in-phase distortion only a), out-of-phase distortion only b).

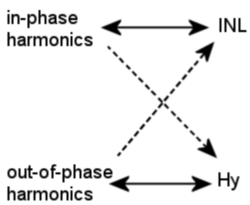


Figure 12. Relation of signal parameters and ADC parameters (INL, output-related hysteresis)

V. Conclusion

The dynamically measured INL is considerably changing with the test signal parameters. Any change of the amplitude and/or the frequency of the signal results in a change of INL. The question is whether the INL testing makes sense for the fast ADC, because the histogram based INL does not represent only the static errors. As shown in [4] the estimation of INL from complex spectrum is possible. However, the estimation of complex spectrum from INL is impossible due to the lack of out-of-phase distortion. Hence, it would be useful to have a complementary characteristic to the INL, some 'imaginary' INL. The output-related hysteresis described in this paper is suitable for this purpose, however it is not perfect because of the distortion of the hysteresis characteristic. In addition, the INL/hysteresis model is valid just for one working point of the ADC (amplitude, frequency). It seems that for fast ADC's the spectral description of ADC nonlinearity (worst case SFDR and harmonic distortion) is more useful, because this description is better related to the ADC applications and the measurement is more simple. Nevertheless, the periodicity of the INL and the hysteresis characteristics can be useful for the determination of a suitable dither level.

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