DESIGN, SIMULATION, AND TEST STRATEGIES FOR ANALOG-TO-DIGITAL, DIGITAL-TO-ANALOG CONVERSION CHANNELS IN WIRELESS APPLICATIONS

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Abstract – In this paper, considering as driving example an analog base-band processor for mobile communications, integrating complete A/D and D/A data conversion based IPs, as transmit/receive base-band ports, voice-audio codecs, auxiliary codecs, we will present an overview of a number of design-for-test, modeling, simulation, and test strategies, aiming to ensure both a complete and economical test of the chip. Our goal will be not only to highlight the effectiveness of a synergic deployment of techniques, like analog design-for-testability (DFT), design modeling, statistical analysis, correlation of electrical parameters, on-chip test overhead (ABIST = Analog BIST), on-board circuit overhead, definition of different test levels and specific test sequence, but also the imperative need to collect and exploit, within the project context, the complete fan of microelectronics "techno-cultures" [1], like design, characterization, test, and product engineering, without which a readily "time-to-market", fully-tested product introduction would be not feasible.

1. INTRODUCTION

The wireless base-band IC domain, thanks to the current proliferation of multi-mode, multi-standard, and multi-service communication systems on one side, and systems-on-chips (SOCs) integration pushing trend on the other side, is experiencing a new wave of high-complexity base-band products. These products, which are based on a number of complete analog-to-digital, and digital-to-analog conversion channels with embedded signal conditioning, will gain further importance in the coming years, as they evolve into more complex systems, to control many different functions. At present, it is expected that the availability of future technologies, such as micro and nano systems, MEMS including integrated tunable resonators as well as other special components, will enable the deployment of the most advanced system architectures, like SDR (Software-Defined Radio), and circuit architectures, like DCR (Direct Conversion Receiver), to design and industrialize user-centric, multi-mode and multi-function, beyond-third-generation (B3G) wireless portable terminals [2]. For the base-band processing part, which contains typically a fairly large number of analog-to-digital, and digital-to-analog conversion channels, like voice-audio codecs, base-band transmit and receive ports, and auxiliary codecs for radio control, for example power amplifier linearization, automatic gain, frequency, and power control, testability becomes a challenge. Economical test is imperative, and its engineering relies on a combination and coordination of different domains of technical expertise, as well as on economic aspects, to be undertaken from the beginning of the design phase.
In this paper, starting from the study of a real case of an analog base-band chip, we will discuss a number of different techniques to put in place, in order to succeed in a cost-effective test of such product, while respecting at same time the necessary time-to-market requirements.

2. WIRELESS AUXILIARY CODECS: DESIGN FOR TESTABILITY CONSIDERATIONS

2.1 Architecture description and design-for-testability considerations

We will start our analysis by considering the architecture of a base-band auxiliary codec. An auxiliary codec, as can be found in base-band chips for wireless communications like GSM, CDMA, PMR (Professional Mobile Radio), or any other standard, is basically composed of: i) one or more A/D converters, possibly with multiplexed inputs, to support battery, temperature, as well as other measurements, ii) several D/A converters, including their respective output buffers (Op-Amps in voltage follower configuration), which can have different characteristics, and are needed to perform some radio control functions, like RX AGC (Receive Automatic Gain Control), AFC (Automatic Frequency Control), TX PWR (Power Ramping), RF PA (Power Amplifier) linearization, and finally iii) a precise reference generator. The auxiliary codec, even if composed of separate converters, due to physical effects and electrical constraints, has to be regarded as a unique entity. For example, given power dissipation requirements, which are very stringent for wireless portable handsets, data converters have to be powered on when used, and powered off when unused with the fastest achievable startup times, and in relation to the particular operating environment, one, more, or all converters can be on at the same time, in a more or less random fashion. The static (INL, DNL, full scale range, offset and gain errors), as well as time domain parameters (settling time, glitches) of the converters, must be guaranteed under any of the above mentioned situations, which mandates a robust design against cross-talk problems, voltage/current drops of the common reference generator, on-chip noise, external noise coupling, and so on [3]. Figure 1 shows an overview of an auxiliary codec, where a number of design-for-testability considerations, are addressed in the design of the IP circuitry.

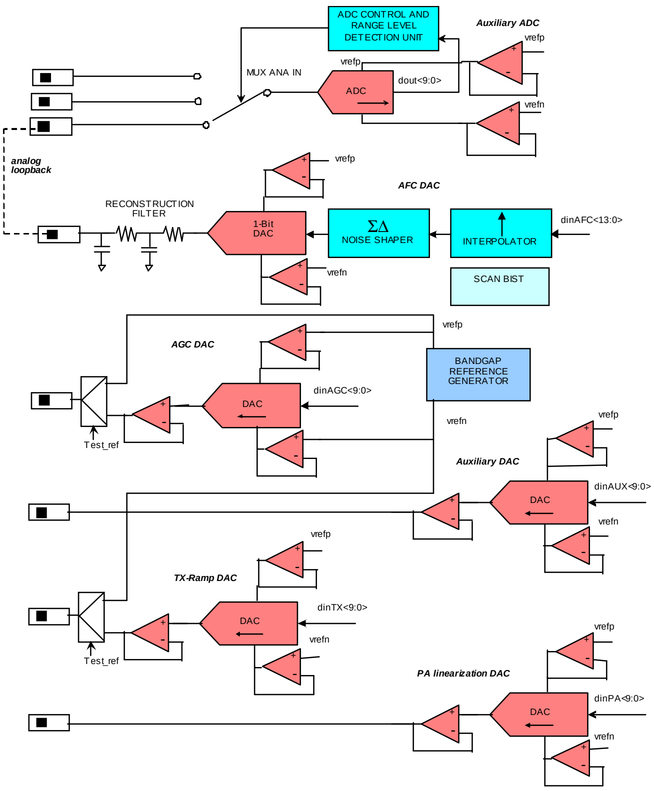

Figure 1. Auxiliary Codec, including dedicated DFT and DFC (Design For Characterization) hardware

Assuming that one goal of the project would be to possibly avoid the use of expensive ATE (Automatic Test Equipment) equipment, containing sophisticated analog stimuli generators and DSP acquisition systems, to favor almost digital testers to test the IP, one could think of adding on-chip some specific hardware to replace the ATE resources. In fact, the choice of going through the integration of an on-chip test core for analog and mixed-signal circuits, providing both input stimuli and output acquisition, instead of a classical test performed by ATE machines with analog generators and DSP analyzers, is mainly dependent on cost considerations. For this reason, the on-chip hardware overhead area for test should be very limited. The integration of purely digital functions to implement the test core, like digital signal generators, FFT processors, is typically inexpensive for SOCs, especially in CMOS deep sub-micron technologies, where the gate density is high. On the other hand, analog functionality, like data conversion (A/D or D/A), filtering, is also required to complete the test core system . For example, to test on-chip an analog-to-digital converter, we would need in the test core system: i) a digital signal generator, ii) a digital-to-analog converter, and iii) a digital signal analyzer, like a FFT processor. The auxiliary codec, given its architecture, represents an ideal situation to implement the on-chip test strategy, in an cost-effective manner, since if good assumptions are made in the design phase, and a correct test flow is established, some analog circuits, which are present because required in the normal operating mode, can be re-used, once their functionality and performance has been verified, as integrating parts of the test core. This is the case for Figure 1), where a 1-bit sigma-delta DAC has been intentionally chosen, to implement the high-resolution AFC DAC. In fact, this architectural choice is satisfying both a specification requirement, as a 1-bit sigma-delta DAC complies well with the need of having high-resolution for the AFC (14-bit in the example), but also a test strategy requirement, aiming to have "on-chip" a high-resolution DAC, to be re-used as generator of precise analog test signals, for example for testing the auxiliary ADC. Moreover, the test of this 1-bit sigma-delta DAC, does not require an expensive analog tester: the digital part (interpolator plus sigma-delta truncator) can be tested automatically by scan BIST, and the analog part, which has a functionality similar to a digital buffer (1-bit DAC with a post-filter), can be verified just with a digital tester (pulses can be sent at the 1-bit DAC input, and the output level, with the expected rise/fall times, can be tested). It can be useful in a product to have the possibility of characterizing the building blocks. In the auxiliary codec of Fig.1 the reference voltages are intentionally not available externally for signal integrity and protection from external noise coupling. Even if the reference generator is indirectly tested through the ADC / DAC converters, by means of their offset (vrefn) and full-scale errors (vrefp), it may be useful, for characterization purposes, to have available externally the outputs of the references. This feature is easily achieved by simply adding multiplexers at some output pads, controlled by a test signal. It should be noted that the pad count does not increase, and the hardware overhead is limited to few muxes and some logic. We can define this dedicated hardware as DFC (Design-For-Characterization).

2.2 *Electrical parameters, simulations and statistical analysis, final test strategy*

Testing just a necessary and sufficient set of electrical parameters, allows to not waste test time, and save cost. In this sense, it is useful to classify electrical test parameters for data converters into different subsets. This is convenient, since an ATE can run one acquisition, for example a spectral analysis, covering a whole set of parameters, i.e. SNR, THD, SINAD, SFDR, without significant additional cost. Table 1 shows a convenient classification of possible subsets. Depending on the application, one, more, or the whole set of subsets must be run on test. In those cases where there is no concern about performance, a functional test is sufficient, enabling the lowest possible cost. For example, one could explore just few points of the transfer characteristic of a data converter to roughly assess its linearity, especially if, during the characterisation phase, which is normally preceding the production test, a reproducibility of the characteristics is found. For what concerns the auxiliary codec, where high precision is required from the ADC in the measurement of the physical quantities like battery voltage, temperature, and from the DACs in the control of the RF radio functions, the static parameters, as well as the time domain parameters, need to be tested to ensure that they are in specification limits. The subset 2, static test, and 4, time domain test, are thus appropriate to achieve the test of the auxiliary codec. A simplified cost saving subset, like the functional test, is considered inappropriate for the auxiliary codec, because risky. One could think of trying to guarantee in spec the INL, DNL, and offset, gain, full scale errors by exploring only very few points of the characteristic; in reality, the random offset of the output amplifiers in the DACs, causes a code-dependent non-linearity, which is also random and very difficult to predict. In the project context, it is important to gradually evaluate and assess the performance of a block before the final production test. This goal can be achieved firstly by an extensive statistical analysis and simulation in the design phase, like the montecarlo simulation, followed by an accurate silicon characterization. Figure 2 shows the results of such statistical analysis performed over the INL of the ADC of Figure 1. All the circuit elements, like transistors, resistors, capacitors, are randomly mismatched, and a number of simulations run over different netlists. The simulated limits are compared afterwards with electrical characterization of the blocks, possibly embedded in the real product environment. As previously discussed, the addition of a very small hardware overhead, like switches, multiplexers, simple logic for digital control, enables this possibility.

Test Level	Subset Name	Parameters Tested	Comments
TL1	Functional Test	Functional Behavior	Few points of characteristic explored. Lowest Cost.
TL2	Static Test	Offset, Gain, Full Scale Error INL, DNL	One DC Test covers all Parameters
TL3	Frequency Test	ENOB, SNR, THD, SFDR	One AC Test covers all Parameters
TL4	Time Domain	Settling Time Startup Time Glitch Energy	Different Tests usually needed.

Table 1. Data converters electrical parameters classification into different subsets.

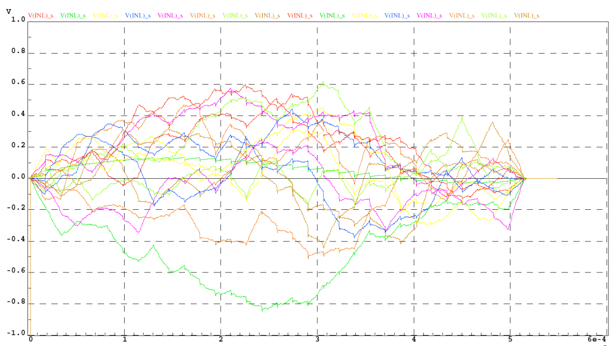

Figure 2. Montecarlo statistical analysis on the INL of the ADC

3. WIRELESS BASE-BAND MODEMS: DESIGN FOR TESTABILITY CONSIDERATIONS

3.1 System description: example with GSM modem

A base-band modem (Fig. 3a)), placed between the DSP interface and the RF part, modulates in transmission an input basic digital bitstream into two quadrature I and Q analog signals, respecting specific requirements of spectral emission, the so-called "GMSK Spectral Mask" , and modulation errors, namely the phase errors (Fig 3b). The receiver performs inverse operations.

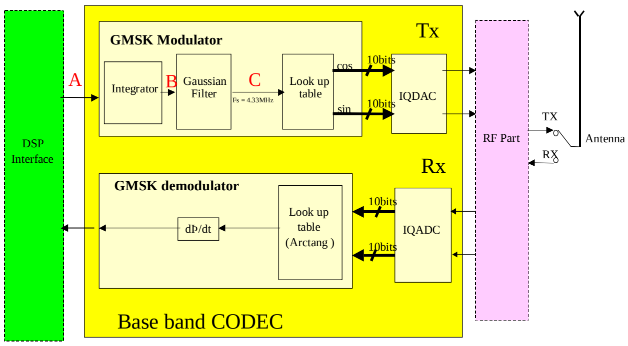

Figure 3a): Base-band modem block diagram

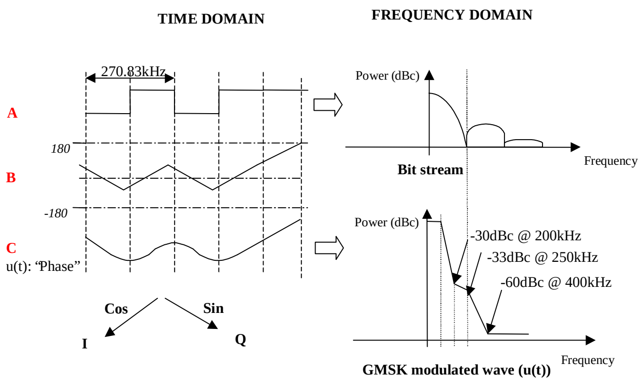

Figure 3b). Time and Frequency domain behavior of signals on the TX channel

3.2 Test Strategy: ABIST (Analog BIST)

For the analog base-band modems, we are potentially in a different situation than the auxiliary codec, as the function must respond to specific system requirements, which are anyway linked to the dynamic performances of the converters (SNR, THD, SFDR,…). For this part, we aimed to explore the feasibility and the cost of embedding an FFT processor on-chip. A complete GSM modem, including GMSK modulator, demodulator, IQDAC, IQADC, FFT processor, RAM data storage, was designed in Atmel AT58K CMOS 0.18um technology. The layout of this experimental chip is shown in Figure 4. The gate count of the FFT machine is around 30kgates, which gives reasonably small area occupation in CMOS 0.18um technology.

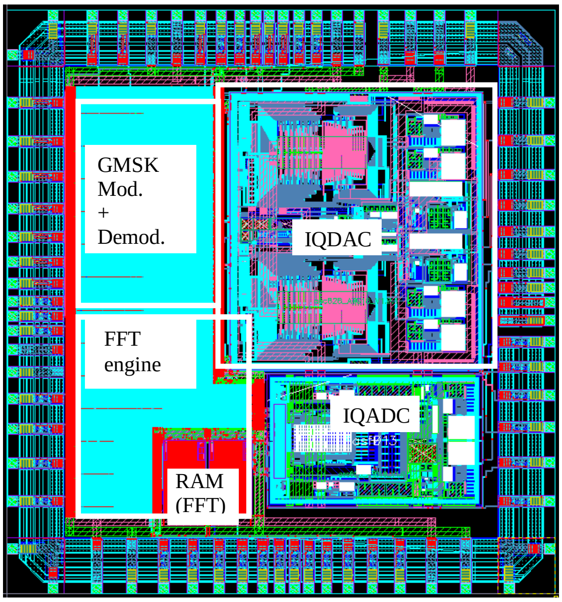

Figure 4. GSM base-band modem experimental Chip with on-chip FFT in Atmel CMOS 0.18um technology

3.3 FFT processor architecture and operation

Figure 5 shows the architecture of the FFT BIST machine. The signal acquisition module stores the input signal in a RAM.

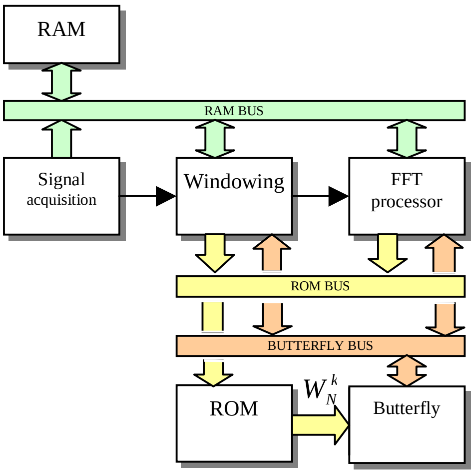

Figure 5. FFT processor architecture

Then a windowing operation is performed, to reduce the discontinuity between the first and the last point of the stored signal.

Finally, the FFT is processed using the butterfly module (Fig. 6), which computes a 2 points DFT. This module contains an optimised complex multiplier using the redundant binary arithmetic, which is twice as fast as a standard complex multiplier for a given area.

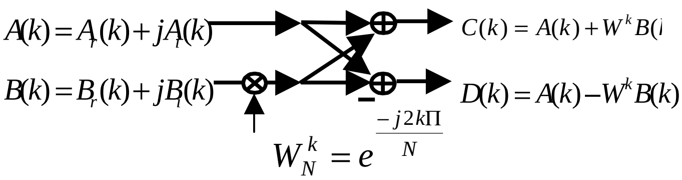

Figure 6. Butterfly module

3.4 Design, Modeling and Parameters Correlations

For the wireless base-band modems, it should be stressed that test of certain system parameters, like the phase error, could be so complex within an industrial environment, that the parameters themselves must be guaranteed by sufficiently robust design. In some cases, correlation can be exploited, if an almost direct relation with another electrical parameter is found. This is the case, for example, for the GSM IQDAC, where a direct relation between the phase error and the cutoff frequency of the reconstruction filters is found. Figure 7 shows the constellation diagram for an IQDAC having fc=200kHz and fc=500kHz cutoff frequency, coming from behavioral simulations. Results show that for fc=200kHz the constellation diagram is highly dispersed. An enough high cutoff frequency, for example fc=400kHz, in worst case condition, has to be chosen in the design phase. The cutoff frequency can then be measured with the FFT machine, to give enough confidence that the phase error is in spec.

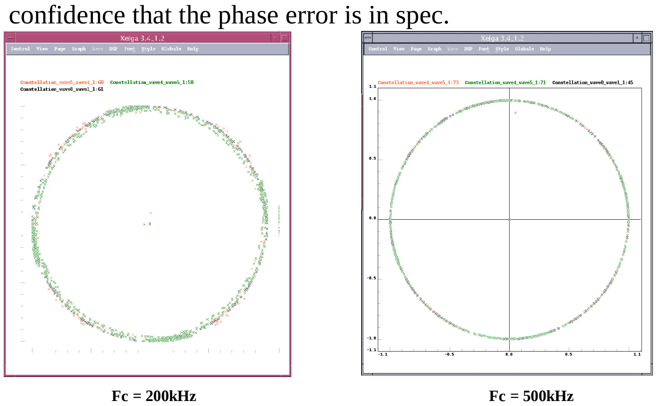

Figure 7. Influence of the IQDAC cutoff frequency over the IQ constellation.

4. CONCLUSION

In this paper we have discussed about a different number of concepts and techniques, which can be very useful to ensure a cost-effective test of products including wireless data conversion channels. The optimal solution, of course, does not exist and has to be defined product-by-product. It can be identified by exploiting, within the project context, a wide range of microelectronics "techno-cultures" : design, characterization, test, product engineering and marketing expertise.

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