

Measuring the DC accuracy of high performance Analog to Digital Converters

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The standard DC parameters of an Analog to Digital converter (ADC) are linearity (integral and differential), offset and gain. To test these parameters, the voltage needs to be measured, as the output of the ADC changes from one code to the next code (transition voltage). For example, the unipolar zero of an ADC is specified as the voltage of the first code transition (code 0 to code 1) minus the respective voltage of half a LSB (least significant bit). This article compares different test solutions.

The easiest way to measure the performance of an ADC is to apply a precise low noise voltage to the ADC input. The transfer function can be monitored by stepping the precision voltage through the input range of the ADC and recording the output of the ADC (see Figure 1).

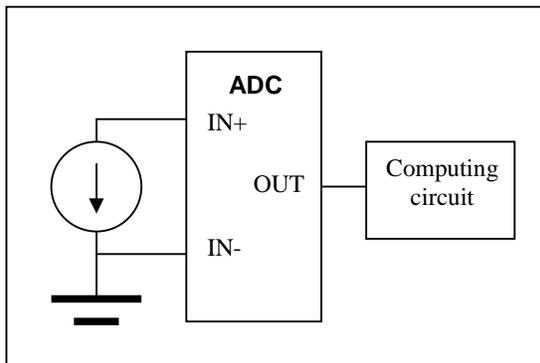


Figure 1: Simple circuit to compute the transfer function of an ADC

Different noise sources (input signal, thermal and flicker noise of the ADC, kT/C -noise of the sample and hold) cause the effect that the transition voltage is unstable. Therefore, the data of the circuitry of Figure 1 is usually analyzed with the histogram method. The actual code length is evaluated by counting the hits of the code of interest and comparing it to the average hits per code.

Usually, a ramp is applied to the input of the ADC. The steepness of the ramp might be chosen, so that there is an average of at least 8 hits per code. The ramp should be repeated often enough so that the influence of the power supply (50/60Hz) as well as noise is suppressed. In the example of Figure 2, there are 4 up and 4 down ramps and during each ramp, there is an average of 8 hits per codes. Figure 2 shows a typical histogram test.

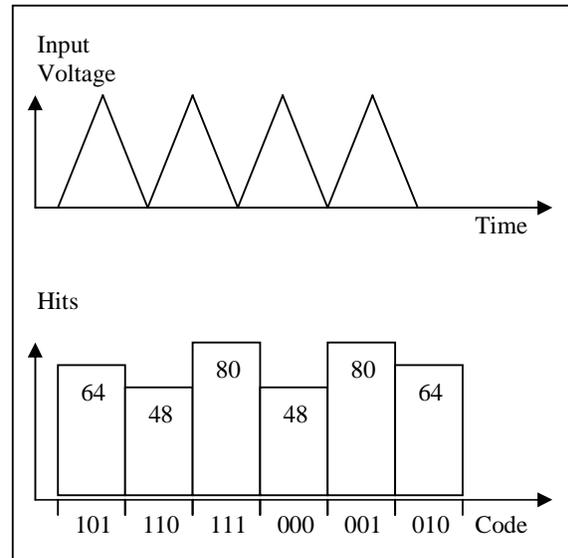


Figure 2: Histogram test

A good choice for a voltage source might be a Digital to Analog Converter (DAC). The accuracy of the DAC should be higher than the ADCs. If the DAC is not calibrated, then every linearity error, offset error or gain error of the DAC adds an error to the transfer function of the ADC. So for higher accuracy, the output of the DAC should be controlled or calibrated with a precise voltmeter.

A precision voltmeter usually captures the input voltage with an integrator and measures over a power line cycle (50 of 60Hz) to terminate the influence of the power supply.

Most ADCs include an internal sample and hold capacitor. After a conversion, this capacitor is switched back to the input of the ADC and causes a voltage glitch. Therefore, an adequate input driver [1] needs to be added between the DAC and the ADC. Also the wiring from the voltmeter to the DAC causes some distortion. The voltmeter should be decoupled with a high precision operational amplifier. (See Figure 3.)

Every amplifier will add some offset, which can be calibrated by measuring a DC voltage directly at the inputs of the ADC first and then over the decoupled

path. During the calibration of the offset, the ADC needs to be turned off; otherwise the glitches mentioned above will add another error.

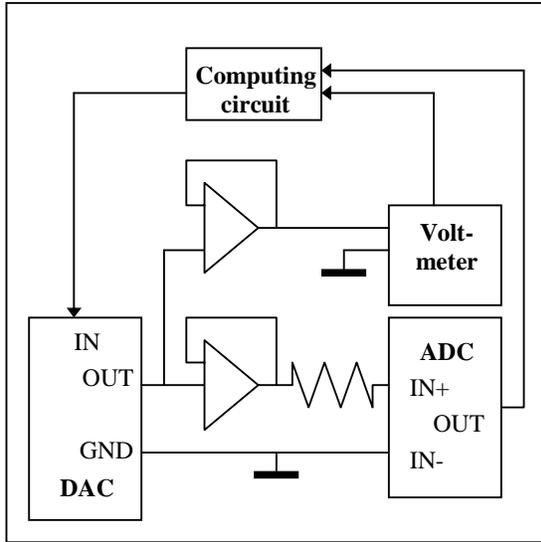


Figure 3: Measurement circuitry including a voltmeter

If the resolution or performance of the ADC is equal or close to that of the DAC, then the test setup is not accurate enough. In which case, stacking two DACs on top of each other as shown in Figure 4 can increase the resolution of the test circuit. The two DAC output voltages are added, using a factor of one for DAC₁, but using a factor divided down by x for DAC₂. Therefore, if x = 128, another 7 Bits of resolution will be added. Since DAC₁ sets the coarse voltage, it is also called the pedestal DAC.

The gain adjustment (factor 1 and 1/x) and the adder of the two DAC output voltages can be implemented with an operational amplifier that is configured as shown in Figure 5. This is mainly an inverting amplifier with two input voltages. The negative input is at virtual ground, so that the input currents are $i_1 = v_{in1}/R_1$ and $i_2 = v_{in2}/R_2$. As the input of the amplifier has high impedance, the current is added ($I_{fb} = I_1 + I_2$) and flows through the feedback resistor R_{fb} . The output voltage can be calculated as

$$V_{out} = -I_{fb} * R_{fb} = -v_{in1} * R_{fb}/R_1 - v_{in2} * R_{fb}/R_2.$$

With $R_1 = R_{fb}$ and $R_2 = x * R_{fb}$, the output of the amplifier is:

$$V_{out} = -(v_{in1} + v_{in2}/x).$$

A capacitor should be placed in parallel to R_{fb} to minimize noise.

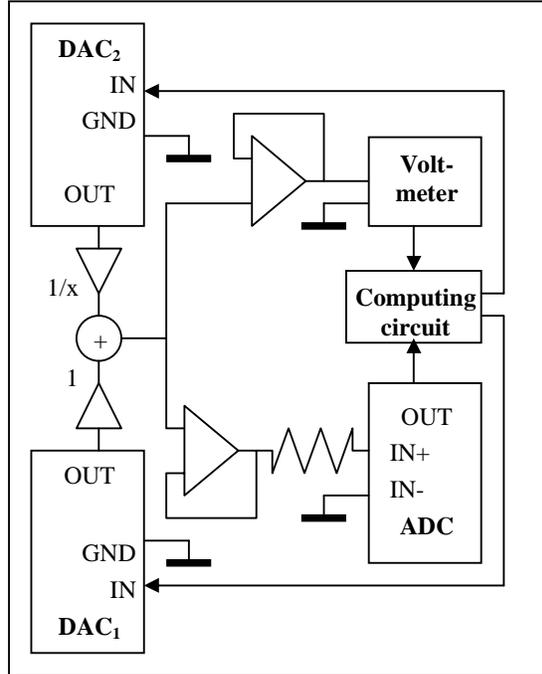


Figure 4: Circuit with two DACs to increase the accuracy

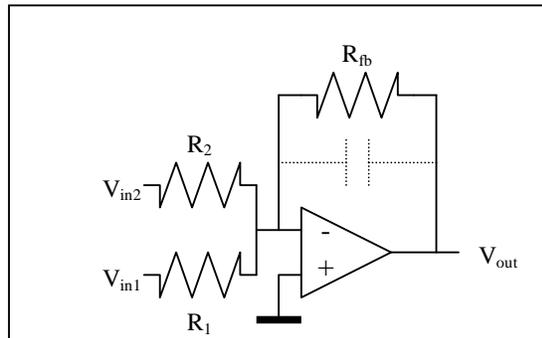


Figure 5: Implementation of an analog Adder

With the setup in Figure 4 it will be difficult to implement a linear and monotonic ramp. So instead of taking the distribution of codes (see histogram test in Figure 2) a simple feedback loop is implemented in the computing circuit, so that the input voltage at the ADC converges to give the transition voltage v_{tr} of the code of interest.

The pedestal DAC is set to the code of interest, so that the input voltage of the ADC is already close to the transition voltage. In case the output code of the ADC is smaller or is equal to the code of interest, the value of DAC₂ now called the servo DAC is increased, otherwise

it is decreased by one step. In this way, the input voltage of the ADC will toggle with very high accuracy around the transition voltage. The integral measurement of the voltmeter will further average the small steps.

This feedback system is also called a servo loop. It has the additional advantage that high precision DACs are not necessary anymore and that the performance of ADCs can be measured with an accuracy that is equal or higher than that of the DAC.

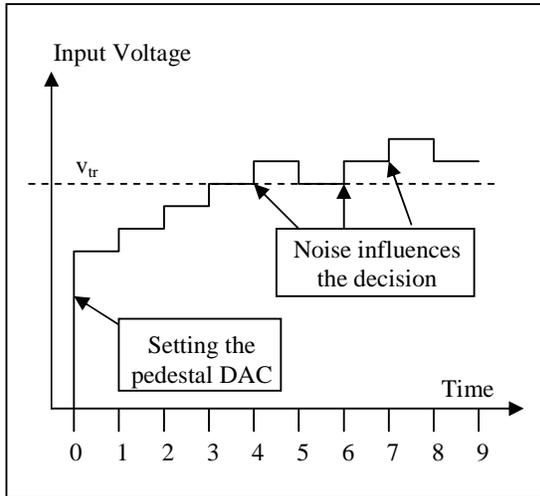


Figure 6: Settling scheme of the servo loop system

Figure 6 shows an example of how the input voltage of the ADC within a servo loop system might work. At time 0, the pedestal DAC is set and applies a voltage that is close to the transition voltage v_{tr} . As the ADC output is still below or equal to the code of interest during the times 1 through 3, the servo DAC increases the input voltage step by step. At times 4 and 6, the input voltage coincides with the transition voltage. The noise of the system will decide if the output of the ADC is equal or above the code of interest and at time 7, the system noise even causes a wrong decision. As soon as the code of interest and the code above both occur at least once, then the integral measurement of the voltmeter can start to measure directly the transition voltage. The integral measurement will average out the system noise and therefore a high repeatability is achieved.

The servo loop circuit can be simplified by replacing the servo DAC with an integrator that adds some voltage to the input, if the output code is above the code of interest, else it subtracts some voltage. An implementation of a system with an integrator is shown in Figure 7.

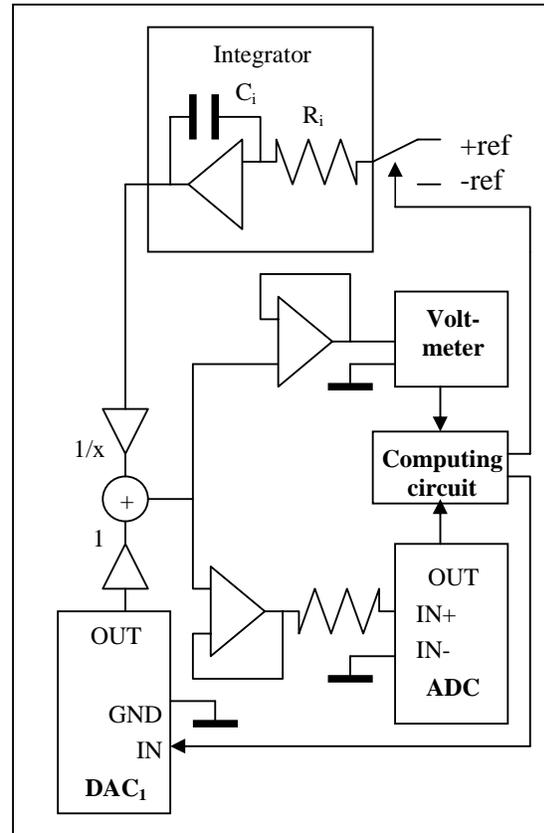


Figure 7: Implementation of the servo loop with an integrator.

A PC might provide the code of interest. The control circuit just compares the code of interest from the PC with the output code of the ADC and adjusts the switch at the input of the integrator. This can be done with a few discrete gates. The PC waits for a while, so that the input voltage of the ADC can settle, and then starts the integral measurement of the voltmeter. After the PC reads the result from the voltmeter, it sets the next code of interest. The software and control circuitry are very simple.

The change of the output voltage of the integrator during a conversion time Δt can be calculated as follows. A constant positive or negative input voltage is applied to the resistor of the integrator R_i . As the node at the operational amplifier is at virtual ground, the input current can be calculated to $I_i = \pm \text{-ref} / R_i$. This current is charging or discharging the capacitor C_i :

$$C_i = \Delta Q / \Delta V = (I * \Delta t) / \Delta V$$

$$\Delta V = (I * \Delta t) / C_i = (\pm \text{-ref} * \Delta t) / (R_i * C_i)$$

So, if the reference is 10V, the conversion time is 2 μ s, R_i equals 100kOhms and C_i is 1 μ F, then

$$\Delta V = 200\mu V.$$

In addition, this integrator output voltage will be divided by factor x . If x is 100, then the input voltage of the ADC changes by only 2 μ V per conversion cycle. In this way, high accuracy measurements are possible.

Taking histograms or making integral measurements or using the servo loop concept all take the advantage of averaging. Some effects like spikes in the middle of a transfer function might not be seen. Therefore, it is always necessary to make the transfer function visible. This can be achieved by implementing a slow ramp (ICs are available on the market) that is added to the pedestal voltage and implemented to the input of the ADC. The ramp is also directly connected to the X input of a scope. The least significant bits of the ADC output are applied to a DAC. The DAC output voltage is applied to the Y input of the scope.

A certain bit of interest (bit i) can be used to offset the DAC output by applying it as the most significant bit (MSB) to the DAC. The DAC can either be a discrete IC (see Figure 8) or it can be implemented with binary weighted resistors.

This article presents different test solutions for the DC parameters of ADCs. They can be measured with a single ramp, a histogram or with the servo loop method depending on the accuracy needed. The histogram and the servo loop method use averaging and therefore some errors in the transfer function might not be visible. Even after measuring the performance with a precise test setup, the transfer function should be visualized with the stair case circuitry. Otherwise, noise, glitches or other things might not be seen.

[1] Frank Ohnhäuser, 'Ansteuern der Eingänge von A/D-Wandlern', Design & Verification 10/2002 page 22-24.
<http://www.publish-industry.net/media/design-verification/dv102002/dv102201.pdf>

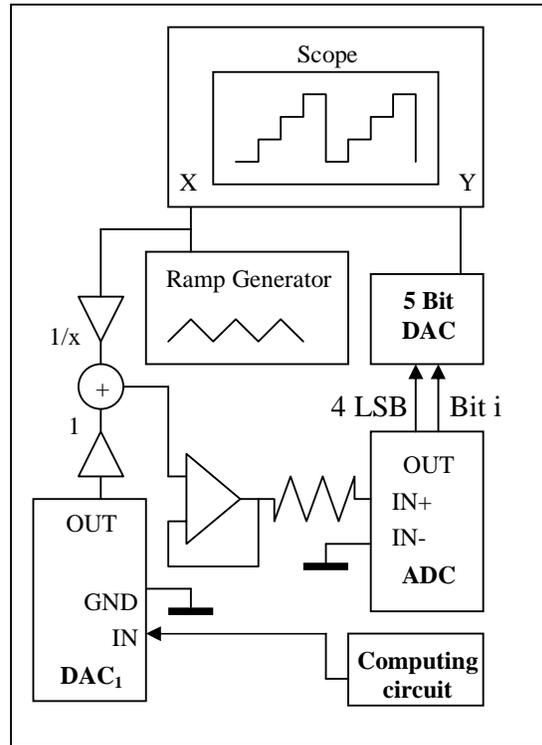


Figure 8: Staircase circuit