A 0.9-V 10.7-MHz 3.6-mW Bandpass $\Delta\Sigma$ Modulator Using Unity-Gain-Reset Opamps

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ABSTRACT—A low-voltage and low-power bandpass $\Delta\Sigma$ modulator is described. In this design, two novel ideas are incorporated: unity-gain-reset and integrating-two-path techniques. A test chip, realized in a 0.35-μm CMOS process and clocked at both 20 and 40MHz, provided a dynamic range DR=45dB and a signal-to-noise+distortion-ratio SNDR=36dB for a 100-kHz signal bandwidth at 5MHz center frequency, and DR=30dB and SNDR=32dB for a 200-kHz BW at 10MHz center frequency. The supply voltage was 0.8 V for 20MHz clock, and 0.9 V for 40MHz clock.

1. INTRODUCTION

Bandpass A/D converters allow the simple and accurate processing of narrow-band signals. Such signal processing is needed for wireless communication systems, spectrum analyzers, and special-purpose instrumentation requiring narrow-band sources.

Recently, there is increasing interest in low-voltage bandpass $\Delta\Sigma$ ADCs [1] - [6]. Low-voltage circuits are required for ICs containing both digital and analog circuits on the same die, where reliability issues may arise due to sub-micron CMOS process, and also low power consumption is needed for the digital circuits. At the same time, higher clock-rate analog-to-digital converters and higher intermediate-frequency modulator/filters are needed for current and future communication applications.

We have previously shown LV implementations of SC lowpass ADCs and low-pass filters [10] based on the *Unity-Gain-Reset* (UGR) technique. We have also described a robust resonator architecture for switched-capacitor (SC) bandpass ADC and filter applications [7] - [8]. We named it the integrating-two-path (I2P) resonator. (This resonator was independently invented and implemented by Salo et al. [9]. In their circuit, the focus was on using a high IF, but with a higher (3V) supply voltage.)

This work describes a LV (0.8-0.9V) band-pass $\Delta\Sigma$ modulator using UGR and I2P stages. When fabricated in a standard 0.35-μm CMOS process, it could be clocked over 20MHz, and achieved a 36dB SNDR performance over a 100-kHz bandwidth. Over a 200-kHz signal BW, it gave SDNR=30dB.

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2. LOW VOLTAGE BANDPASS $\Delta\Sigma$ MODULATOR

The bandpass $\Sigma\Delta$ ADC can be easily designed by starting with a lowpass $\Delta\Sigma$ modulator and then performing a lowpass to bandpass transformation by the change of variables $z^{-1} \rightarrow -z^{-2}$. This transformation maps the zeros of the lowpass $\Sigma\Delta$ Modulator to $f_s/4$ and $3f_s/4$, suppressing the quantization noise around those frequencies. Hence, a fourth-order bandpass $\Sigma\Delta$ modulator is obtained from its second order lowpass counterpart. The resulting output signal of the bandpass modulator is given by $Y(z) = z^{-4}X(z) + (1+z^{-2})^2E(z)$.

The block diagrams of the model lowpass and the resulting bandpass $\Sigma\Delta$ modulators are shown in Fig. 1. Note that instead of a subtraction, there is an addition on the inner loop of the bandpass modulator. Also, instead of integrators, resonators are used to realize the loop filter of the bandpass $\Sigma\Delta$ modulator.

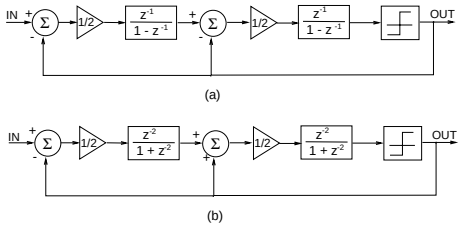

Fig. 1. Block diagrams of (a) a second order lowpass and (b) a fourth order bandpass $\Delta\Sigma$ modulator.

A fourth-order bandpass $\Delta\Sigma$ modulator using I2P resonators is shown in Fig. 2. This modulator uses a pseudo-differential configuration for LV operation. The digital circuit blocks and comparators are not shown for simplicity. The output samples of the upper and lower paths are interleaved.

3. LOW-VOLTAGE OPAMP

A modified version of the opamp used by us for a LV lowpass modulator [11] was used for this bandpass $\Delta\Sigma$ modulator. It is shown in Fig. 3. The resistor was eliminated from the compensation branch of the earlier circuit, and the LHS terminal of the compensation capacitor C_c is connected to node A. This way, a fast forward path is introduced. The gate terminal of the pmos mirror $M11$ is also connected to node A. This change improves the slew-rate performance of the

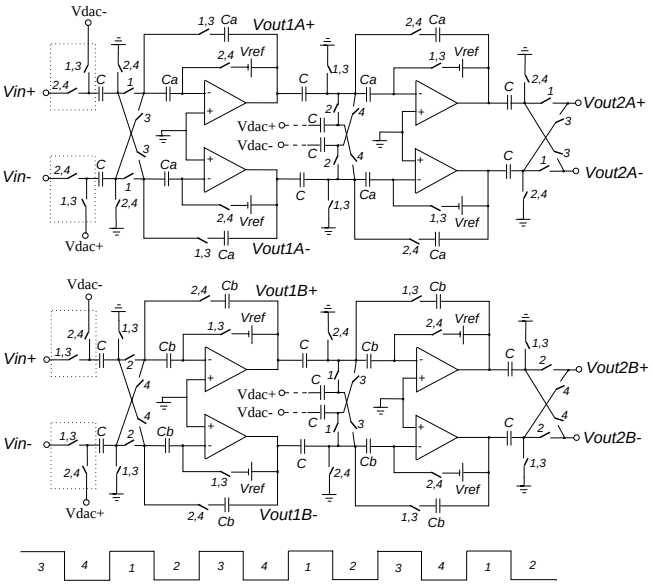

Fig. 2. A fourth-order bandpass $\Delta\Sigma$ modulator.

opamp, since $M11$ now follows the signal.

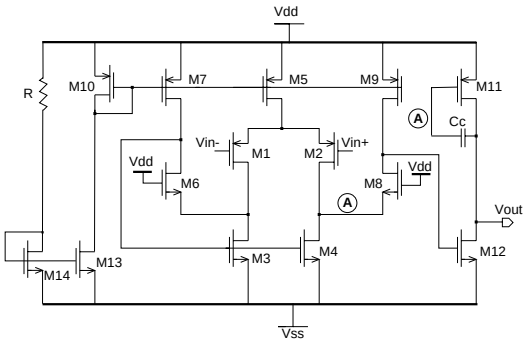

Fig. 3. The low-voltage opamp for the Bandpass $\Delta\Sigma$ modulator.

A design goal was to reduce the power consumption when using the proposed resonator. This was achieved by maintaining the high performance of the LV opamp when the reference current is reduced.

4. MISMATCH EFFECTS IN THE LOW-VOLTAGE I2P STRUCTURE

In the two-path I2P structure, there are four possible mismatch problems, caused by path mismatches, input sampling-capacitor mismatches, sampling clock-edge mismatches, and the offset voltage mismatches of the opamps. These effects will be discussed next.

4.1. Path Mismatches

Path mismatches occur between the multiple paths from the input to the output. There are two paths in the LV I2P resonator, as shown in Fig. 2. Component mismatches will create an attenuated image of the fundamental tone, at the same distance from the center frequency, but on the other side [12]. This tone is called a mirror image. It will be suppressed by the gain of the resonator, since the mismatches affect only the output signal of the resonator.

4.2. Input Sampling-Capacitor Mismatches

The input sampling-capacitor mismatch is reduced in our design by using the same capacitor for sampling both the input signal and the DAC feedback one. This shifts the error signal due to the input capacitor mismatch to inside the $\Delta\Sigma$ loop. Thus, about 20dB of mirror image suppression is achieved.

Simulations were performed with a 1% capacitor mismatch between the paths. Fig. 4(a) shows the Fourier transform of the output signal when the input sampling capacitor of path A is equal to $(1 - 0.01) \cdot C$ and the input sampling capacitor of path B is equal to $(1 + 0.01) \cdot C$. Both DAC capacitors are assumed to be equal to C. Fig. 4(b) shows the spectrum of the output signal when the input sampling capacitor of path A is $(1 - 0.01) \cdot C$ and the input sampling capacitor of path B is $(1 + 0.01) \cdot C$. DAC feedback signals are applied through the input sampling capacitors during the next phase. Better performance is now obtained, since the mismatch is shifted inside the loop, and thus suppressed.

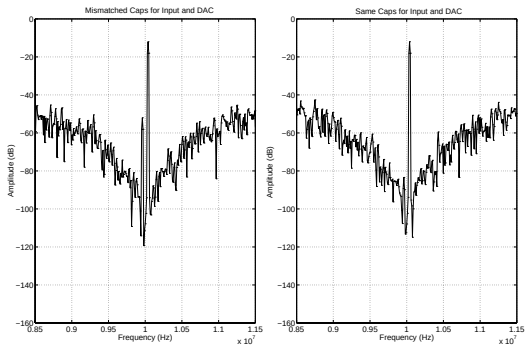

Fig. 4. Simulation results with 1% capacitor mismatch when (a) C_{dac} is separate (b) C_{dac} is the same as input capacitor.

4.3. Clock-Edge Mismatches

Another mismatch effect is due to clock-edge variations (timing skew) between consecutive clock phases ($1, 3$ and $2, 4$). These introduce variations of the sampled-signal amplitude from one path to the other. Doubled clock frequency is used to sample the input signal to the two paths with the same time intervals. Using this clock signal, series switches (one for each signal path) were added, which are turned on/off by this faster clock as shown in Fig. 5. This reduced the skew effect significantly.

4.4. Modulation of the Opamp Offset Voltages

Another problem which may occur specifically in the LV I2P bandpass $\Delta\Sigma$ modulator is the modulation of the offset voltages and the $1/f$ noise voltages of the opamps into the passband. The LV I2P architecture has four opamps per resonator as shown in Fig. 2; hence, any offset mismatches between these opamps will appear at the output once in every four clock cycles. This effect will introduce a tone at f_s/4.

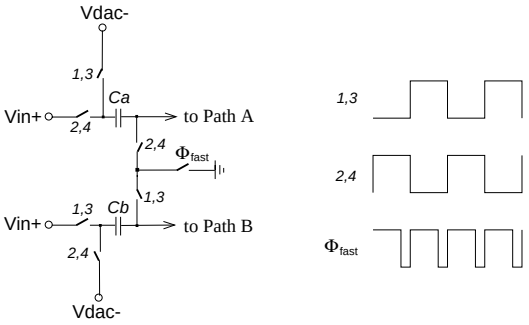

Fig. 5. Solution of the timing skew problem between paths

Simulations show that the bandpass $\Delta\Sigma$ modulator is highly susceptible to first-stage offset voltages. The simulations were done with a 1% capacitor mismatch and with random offset voltages up to 15 mV at the inputs of the opamps. The results are shown in Fig. 6 with and without the use of correlated double sampling (CDS). The tone level at $f_{clock}/2$ is only about

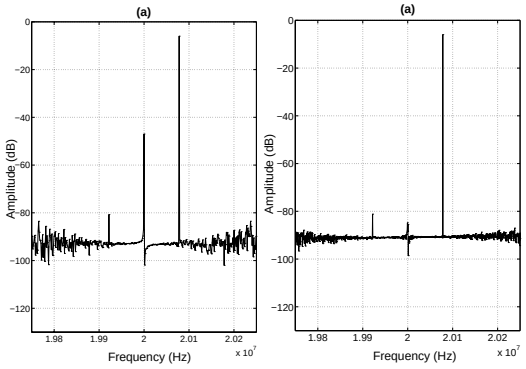

Fig. 6. Simulation results with 1% capacitor mismatch and offset voltages up to 15 mV for 2^{17} FFT points within a 500 kHz frequency interval (a) before CDS (b) after CDS

40dB below the signal level without CDS. Hence the CDS techniques described in [8] was implemented using one additional capacitor in front of each opamp, as shown in Fig. 2. This reduced the tone by an additional 40dB.

5. LAYOUT AND FLOOR PLAN

The prototype IC die photo is shown in Fig. 7. The chip is realized in a 0.35 μm CMOS process. The layout is aimed at achieving symmetry between the pseudo-differential halves. Having the two signal paths close to each other was also an important concern. For this reason, analog cells were mirrored around the horizontal symmetry axis, and laid out as close to each other as possible. The other less-critical parts of the system, such as the switches and digital cells in the two paths, are farther away from each other.

Another important issue is the layout of the clock generation and distribution circuitry. The clock signals should have the same delay to both paths in order to avoid timing mismatches. For this reason, the clock generator is placed in the center of the layout, to the right of the modulator. There are

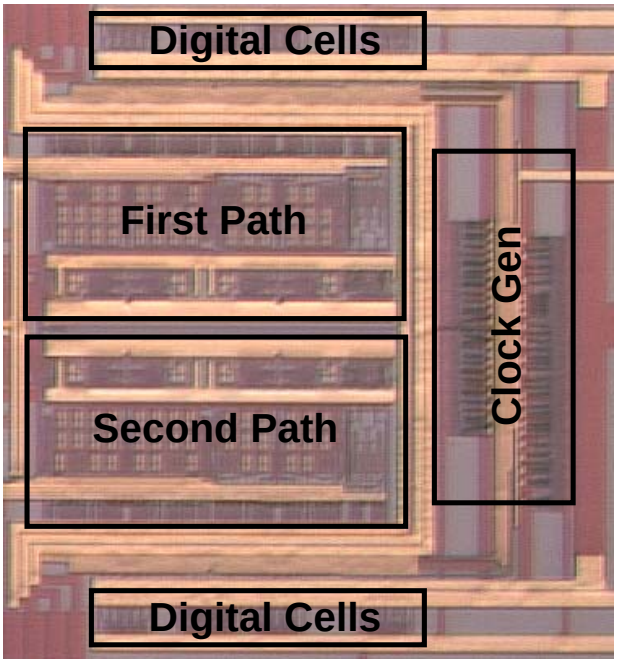

Fig. 7. The drawing of the LV fourth-order Bandpass $\Delta\Sigma$ modulator.

only the comparators on the right side of the modulator, and hence the clock generator will be far away from the critical input nodes. Well separation and ground connections to substrate are placed between the clock generator and the other parts of the system for isolation.

6. TEST RESULTS

The fabricated chip was tested with both 20MHz and 42.8MHz clocks, and with varying (0.8-0.9V) supply voltages. Table 1 gives a summary of the measured results and a comparison with other state-of-the-art LV BP modulators. The typical measured spectrum of the digital output stream is shown in Fig. 8. The SNR and SNDR performances are shown in Fig. 9, while the two-tone test result in Fig. {10.

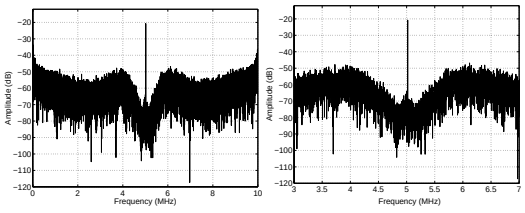

Fig. 8. The spectrum of the digital output stream for 5 MHz center frequency

7. CONCLUSIONS

A low-voltage IF bandpass analog-to-digital converter was implemented in a fully-integrated form. Using novel circuit design techniques, reasonably good performance was achieved down to the 0.8-V supply voltage levels.

Ref. index	Type	Area $[mm^2]$	VDD [V]	SNR [dB]	SNDR [dB]	DR [dB]	PD [mW]	Fclk [MHz]	Fo [MHz]	BW [kHz]
[1]	2^{nd} DT	1.5 (0.5μm)	1	42	—	45	0.24	1.8	0.4	20
[6]	2^{nd} DT	1.3 (0.35μm)	1	—	42	57	12	21.4	10.7	200
[2]	2^{nd} CT	2.9 (1.5μm)	1.2	—	45	40	2.1	4	1	20
[3]	4^{th} DT	2.1 (0.25μm)	0.8	—	61	68	2.5	5	1.25	30
[4]	2^{nd} CT	0.36 (0.18μm)	1.8	51	51	53	1.75	20	2	1000
[5]	2^{nd} DT	1 (0.18μm)	1.8	—	80	95	75	37.05	10.7	9
[this work]	4^{th} DT	0.88 (0.35μm)	0.9	34.7	32.4	30	3.6	42.8	10.7	200
[this work]	4^{th} DT	0.88 (0.35μm)	0.8	35.7	35.4	45	2.4	20	5	100

Table 1. Performance of state of the art SC bandpass $\Delta\Sigma$ modulators

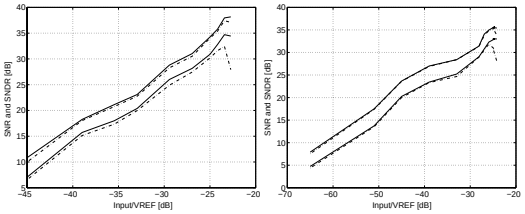

Fig. 9. The SNR and SNDR for (a) 10 MHz (b) 5 MHz center frequencies

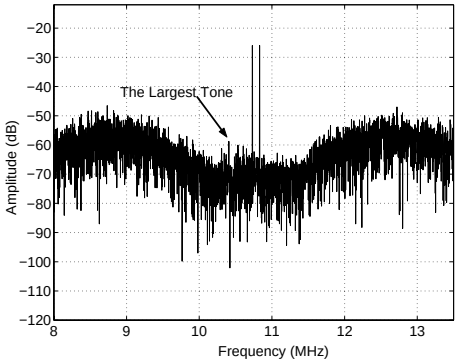

Fig. 10. The two-tone test

8. ACKNOWLEDGMENTS

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