High frequency & resolution ADC : Trends and Modeling

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Abstract : The analog to digital converter is one of the key devices for future receiver design taking into account performance and cost. Is this dream for true software radio applications (within certain conditions) achievable in a few years ?
Developing such application will mean very high analog input intermediate frequency with wide bandwidth to be converted with very low spurious intermodulation (much better than – 85 db) translating to 12..14 bit resolution ADC sampled at very high clock rates.
Modeling of such a specification gives special restriction on the choice of the ADC architecture and process. It can be proven that the only architecture suitable for this future radio application is a massive parallel structure. Introducing such a high linearity ADC without any feedback loop needs new parallel DC and AC linearisation in the analog core to correct mismatching.
The choice of the process to use is an other key: CMOS, Bipolar, BiCmos processes have been studied. Taking into account high frequency clock and analog inputs, high resolution, low noise and low power, only BCMOS of Bipolar (with Vpnp) featuring a high Ft and good matching of components are good candidates.
Several ADC have been realized or simulated : starting from 10 bits 1 Gsps or 2Gsps to 14 bits 200 MSPS with Bicmos or Bipolar process with an Ft of 25 or 75 GHz (SiGe).

Keywords: Software radio, Digital receiver
Pipeline ADC, Flash ADC
Folding and interpolation ADC
Dithering

1) Introduction:

The trend coming from the past years is to lower the number of components in the critical analog receiver chain and in the same way increasing the complexity of the analog to digital conversion and digital signal processing (see fig 1). Following that trend only a few and necessary analog components could be kept in the receiver part and using the software flexibility and increasing power computation of DSP what we call Software radio could be achievable.

This well adaptive concept will be clipped in fact mainly by the physical performances of the ADC. A lot of system (Radar, Telecommunication...) would like to use this ADC as direct down conversion between 1..2 Gsps in the second or third analog Nyquist zone. The requirement of such a system means generally very good SFDR in a very wide analog bandwidth of interest : 12 to 14 bits resolution i.e. -85dB to –95dB with band of a few 100 MHz around the IF (for the multi channel selection).
Is such ADC feasible and what could be the trade offs ?

A lot of different ADC architectures exist now and almost every day new concepts are introduced so we will limit our investigations only to proven high resolution and high speed converters. In fact architectures of ADC are mainly linked with the choice of the process :CMOS, bipolar and Bicmos .
Here is a table explaining the main parameters of each process and the possible key structures which are used in analog design.

	CMOS	Bipolar or Bicmos
Gm	Low in strong inversion : Gm good in weak inversion. dependant of all parameters :area, current ;temp	Always High, only dependent of Temp and current
Number of decade for Current in analog	2 (dependence of area)	10 (no dependence of area)
Matching differentia l pair	10mV	<1mV
Ft	Up 150GHz minimum size and largest current : not usable in analog design ! !	Up to 150 GHz (SiGe) Usable in analog design
Thermal noise	High because low Gm Take care of poly gate resistance	Low because high Gm Take care of base resistance :SiGe preferable.
1/F noise	High Dependence of Length	Very low : A few 1Khz..10 kHz.
Switch in voltage	Easier : Good Switch cap design	Not possible
Switch in current	Not Easier but possible.	Easier
Very high linear opamp (>80db)	Yes	Yes if Bipolar with Vpnp Yes if Bipolar+CMOS No if single NPN (limited 70db)
Ultra low voltage design	Yes	Not easy if single Bipolar Yes if Bicmos.

Table 1 : CMOS/Bipolar Comparison

2) Architecture using Cmos Process.

Using standard Cmos process (with analog option :Poly resistance and Double poly capacitor) several kind of ADC architectures exist : Pipelined, Flash and folding and interpolation. Sigma delta ADC for the time being are limited in term of effective clock rate and useful analog bandwidth so this is the reason why this will not be treated in this article.

2-a) CMOS Pipelined ADC

The most popular one in term of linearity performance seems to be the pipelined ADC one thanks to the intrinsic good matching characteristics (11..12 bit accuracy) of double poly capacitance switch capacitance techniques autocalibration are used to improve linearity. Good results have been showed especially for base band ADC (Ref 1,2,3,4).
The main drawback of such an architecture is the limitation of analog bandwidth with high linearity and clock speed: only baseband ADCs are available: limiting the analog bandwidth and clock rate in the order of several 100 MHz.
Using better process could not solve completely this drawback. By using a better process the supply voltage will drop dramatically with the consequence that the maximum analog input range will drop also but with a larger ratio..
The signal to noise ratio (excluding Harmonics) is proportional to : $\sqrt{KT/C}$
where K is Boltzman constant, T temperature, and C the equivalent load capacitance of sample and hold.
If the analog input is decreasing by a factor of two (which would be the case if with we go from a 0.35um(3.3V) to 0.18um (1.8V) process) the capacitance will be increased by a factor 4. Now if we want to keep a good static and dynamic linearity the dynamic current necessary to track and hold the signal will increase in such a way that the total power dissipation will be much higher than with previous CMOS processes.

Increasing the clock speed is not straightforward because of the intrinsic settling time limitations of the switch capacitance track/hold. One solution could be to interleave several ADCs together (Ref 5,6). Interleaving has a cost : large area and power dissipation (N ADC working in parallel), several external or internal calibrations are needed : offset, gain, time aperture delay (difficult to handle especially for the consumer market).
The main constraint is coming also from the difficulty to match the roll off of the different bandwidths of each ADC core which is limiting very high analog bandwidth with high resolution ADC.

2-b) Flash and Folding/interpolation CMos ADC

The Flash Architecture and the folding/interpolation are a massive parallel concept which are by construction the fastest architecture which allow ultra high clock rate up to 2 Gsps even in CMOS.
The main limitation is coming from the matching of the input comparators due to the very poor matching of Nmos/ Pmos differential pairs.
This matching error is affecting directly against the DNL / INL DC performances. Increasing the component area will help but will increase the equivalent input capacitance to be loaded by a sample/hold or amplifier and thereby limiting the settling time and clock rate.
Several solutions have been proposed to lower this effect : averaging techniques (ref 7,8).
A very high speed ADC (>500 Msps) can be found with a maximum resolution of 6 bits. Here improvements in speed have been shown with better CMOS process (0.18um) with the gain of good power dissipation(Ref 9,10,11).Using better process has the advantage that matching of transistor will improve as it is dependent of the oxide thickness of the gate transistor.

The resolution using this architecture is limited to 10 bits (Ref 12) with low clock rate (<100 Msps) higher resolution seems for the time being very difficult to handle coming from the bad matching of Nmos/Pmos while such resolution appears to be handled with pipeline ADC.

3) Bipolar ADC Converter :

The architecture of high resolution ADC converters is mainly dependant of the advantage that the process gives to the design: in bipolar the main advantage are the high transconductance gm, the speed of the cell, the high available FT and the matching of components.
If very high resolutions are needed a true complementary Vertical PNP or MOS transistor (PMOS) is necessary to achieve a high resolution amplifier otherwise the maximum linearity of such an amplifier (or Sample/hold) could be limited to 10..11 bits (Ref 13,14).
For bipolar or Bicmos ADC several architectures are used : multisteps, flash and folding and interpolation.
The multisteps architecture fit very well for high resolution ADC but with low clock rate (ref 15) :The drawback of such architecture is the limitation of the settling time of the different residue DAC. The advantage of such a design is that calibration to correct INL between segment (during wafer test) can be handled with fuse (if available) or laser trimming..

3-a) Pipeline folding and interpolation ADC :

As explained previously, flash architecture and folding and interpolation (Ref 15) are the fastest architectures in term of speed (>2Ghz) with medium resolution (10 bits).Increasing resolution could be achieved via pipelined folding and interpolation architecture (Fig2) :each folding stage is determining k bits from the most significant bit (first folding stage) to the least significant bit (last folding stage).As explained in the following table this pipeline folding and interpolation ADC core should be designed in terms of DC linearity (DNL and INL) and settling time. The other AC part will come from the input stage : the sample/hold which will handle the very large analog input frequency and high clock rate and equivalent input noise.

limitations	**Sample/hold**	**Analog ADC core**
Thermal Noise	Yes (main part)	Yes (Small part) only first folding stage
-3dB bandwidth (Cut)	YES	NO
Effective analog Bandwidth :	YES	NO : Give only static part
Clock Rate	YES : Track to Hold mode Hold to Track mode	Yes :Settling ADC core
DC linearity	NO : Only large signal THD Typically Second and Third	YES : DNL+INL
Internal Jitter	Yes : coming from input clock stage	No

Each of these limitations are part of the signal to noise formula SNR:

$$20Log\left(Veff / \sqrt{\left(Vacth^2 + Vq^2 + Vdcdnl^2 + Vjitter^2 + Vth^2\right)}\right)$$

Where Vacthd is the rms. value of the combined effect of dynamic and static INL.
Vq : Quantization noise
Vdcdnl : is the rms value of the dnl.
Vjitter : is the equivalent input noise jitter of the clock combine with the analog input frequency.
Vth : is the equivalent input thermal noise (rms.).

3-b) Thermal noise :

As explained before the thermal noise could be considered coming from the Sample/hold input stage. The first stage of the ADC core will account for a small amount to the contribution.
To calculate the thermal noise we are considering figure 3 as a typical track/hold schematic.
The Track/hold has two phases : The first one is the track mode where we will consider only the total integrated noise from the input Vin to the load capacitance Vc. The second phase will be the Hold mode where the total noise will be from input Vc to the output Vout.
Nt is the total integrated noise phase track mode, Nh is the total integrated noise phase hold mode.

$$\text{Ntotal} = \sqrt{(Nt^2 + Nh^2)}$$

In all the chain the gains are considered as unity.
If a sample hold is used we should multiply by √2, If a differential input is used we should also multiply by √2.
The noise density in track mode considering all transistor have the same size and current :

$$Veqt^2 = 4KT * (n\,Rb + n/2gm + (n-1)/(2Bgm))$$

Where n number of components, B=Ft/f.
The total integrated noise is (considering Fcut=Gm/2*pi*cload

$$Nt^2 = KT\,(nRb*gm + n/2 + (n-1)/2B) / Cload$$

We can consider also that the equivalent Noise input resistance of the Track/hold is :Req = (n Rb+ n/2gm + (n-1)/(2Bgm))
Generally we can considered that Nt=Nh so :

$$\mathbf{Ntotal^2 = 2KT * (n\,Rb + n/2gm + (n-1)/(2Bgm))\ (eq1)}$$

Figure 1 :Typical Rx TX software Radio

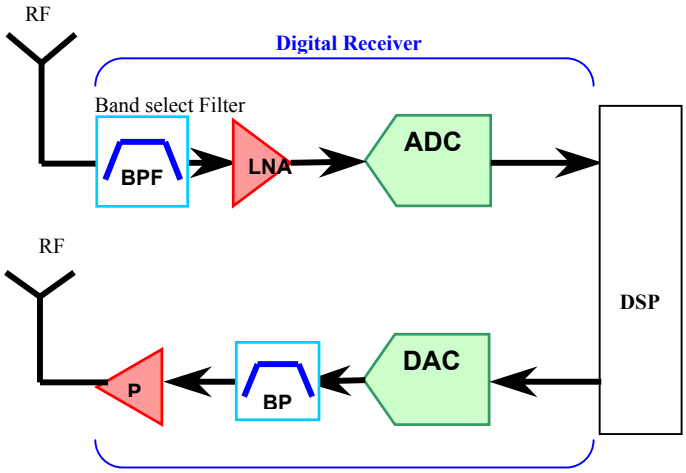
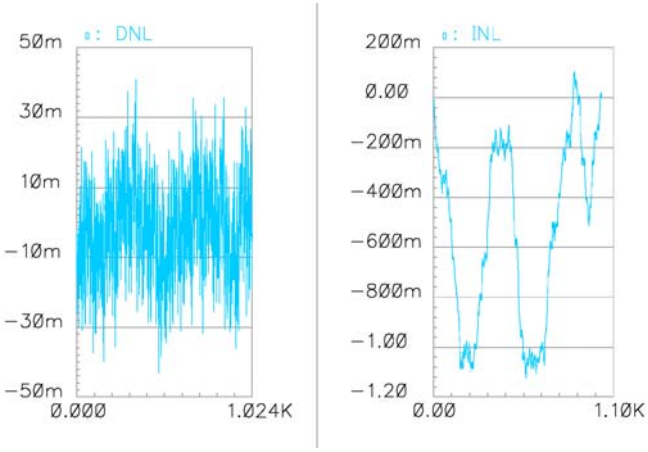


Figure 4 :10 bits DNL/INL with MonteCarlo



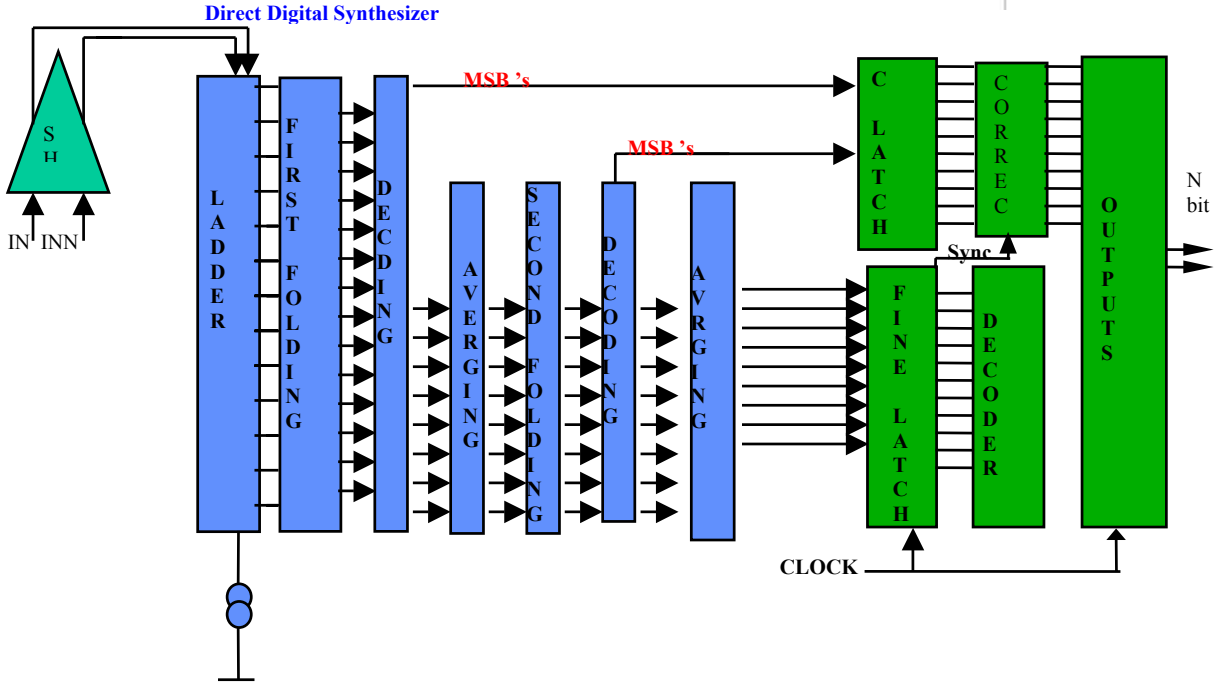
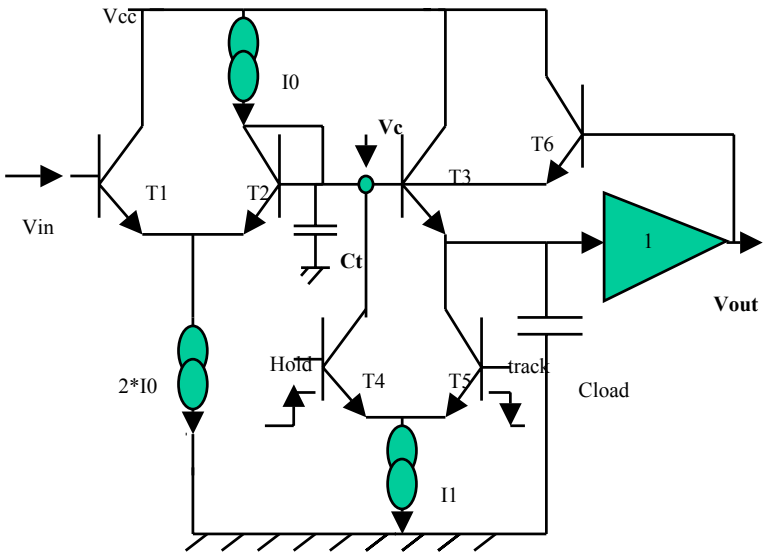


Figure2 : Pipelined folding ADC architecture

Figure 3 : Switch current Track/hold



3-c) Dynamic aspect of track/hold :

In order to handle settling time, accuracy ;track to hold and hold to track mode we can model the track/hold with the following equations :

$$Ct/Gm1 + Cload/Gm3 < 1/(2*Fclock*nLn\ 2) \quad (eq2)$$

$$I0>Max(Ct*4A*Fclock,Ct*2*\Pi*Finmax*A) \quad (eq3)$$

$$I1>Max(Cload*4A*Fclock,Cload*2*\Pi *Ginmax*A) \quad (eq3)$$

$$I1-I0 > Ct*\Delta v/\Delta t \quad (eq4)$$

Where n resolution of the ADC,A amplitude of the analog signal , Ct equivalent parasitic capacitance on node Vc, Δv is the minimum voltage necessary to switch transistor T6, Δt is the rising/falling time of clock.

The following table 3 shows the best estimation of two ADC 12 bits running on a 25GHz BiCmos process:

	12 bits 500Msps Clock 500 MHz Fin	12 bits 1Gsps Clock 1GHz Fin
THD	-80dB	-80dB
Equivalent Noise resistance	44.5	18
Number of T/H	1	2
Cload	5pF	10pF
ENOB(T/H only) Excluding Jitter	11.0	11.0
Power (5V supply) Track/hold only	500mW	4.5W

From this table we can conclude that an ideal ENOB for very high resolution and frequency should not be considered as the key parameter : In fact ENOB will be clipped due to thermal noise and input jitter clock considerations. These noise sources could be seen as white noise so using special digital filtering (averaging..) the true signal can be recovered even under these noise floor so that only THD and SFDR could be the key parameter .

Playing with better BiCmos or SIGEMOS process will help mostly by achieving higher clock and analog frequency and also to a lesser extend a better SNR (lower base resistance, parameter B higher).

4) Analog Core

The analog core is based on multi pipelined folding architecture.
This block will be designed in such a way that only static characteristics and settling times are considered.
Each folding block will give two kinds of bits : Coarse bits which are going directly on to digital core and fine interpolate bits which are loading the next folding block :This process is reapeted until the correct resolution is achieved.
The DC errors of such architecture will come from the combination of mismatching errors coming from each folding block (for instance a pipelined factor of 3) :

$$INL(rms)=\sqrt{\left(\sigma_1^2+\sigma_2^2/G_1^2+\sigma_3^2/G_1^2G_2^2\right)} \quad (eq6)$$

Where σi are the equivalent input matching and Gi the equivalent gain of each folding block amplifier.
Eq6 is showing that mainly the first folding amplifier is limiting the DC accuracy. Typically Bicmos or SiGemos process gives equivalent matching factors of NPN pair between 0.2mV and 1mV for an emitter area of 1um2. Choosing the best factor will be limited by the process of INL performances between 10 bits and 12 bits accuracy.

To improve this new averaging (simple or double) and gain, compensation techniques have been designed (Patents pending)in such way that the equivalent matching of each comparator is divided by 0.6 (simple) or 0.36 (Double) .
Figure 4 is showing DNL/INL simulation using a Monte Carlo analysis on a 10 bits 1Gsps ADC with a matching factor of 0.5mV, a pipeline factor of 2 and simple averaging. The Maximum INL will be within +/- 0.5lsb and thanks to the folding structure DNL will be much less than +/- 50mlsb !!
But these techniques of averaging are not enough if SFDR better than -80db is needed : The best way to improve that is by adding dither noise in a given band (not used in the application) and by filtering it in the digital processing or in the die.
Simulations and experiments (ref 16) have shown that gain of 15..to 20 dB improvements in the SFDR are realistic.

Conclusion : Going to True software radio using ADC as a direct IF Sampler implies that the fastest ADC architecture must be used in conjunction with the fastest silicon germanium with CMOS device. This process should also have a good matching factor for the NPN components. The architecture should avoid any feedback solution technique and use a full and massive parallel solution as the pipelined folding structure. Going to IF sampling means that only SFDR,THD requirements are needed and parameters such as thermal noise and clock jitter should be less significant (white noise) and given in such a way that true signal could be recovered under the noise floor with the best possible distortion: Adding on die dithering could be one of the solutions.

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From 1992 to 2000 he worked at Philips Caen on low power high resolution analog to digital converter for portable or imaging application .Since 2000 he works for ATMEL Grenoble on ultra fast ADC low power and high resolution ADC. He holds 16 patents in the area of ADC architecture.