DESIGN CONSIDERATIONS FOR SDMs BEYOND ADSL

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ABSTRACT †1

This paper presents design considerations for ΣΔMs aimed at high-linearity, high-speed A/D conversion. We analyze the performance of a family of high-order cascade multi-bit architectures in a low-voltage, deep-submicron scenario. We show that, after proper architecture selection, guided by a simple power estimation method, these ΣΔMs are promising candidates to achieve post-ADSL performances in future CMOS processes.

1. INTRODUCTION

Although specifications for broadband access data converters (12−15bit at 1.1−12MHz) seem a priori better suited for pipeline ADC, these converters are not linear enough for some modulation techniques, specially in low-voltage scenarios. On the contrary, sigma-delta modulators (ΣΔM) exhibit high linearity with relatively simple circuitry, which render them worth exploring for the chipset of wireline modems [1] - [8].

Given the large bandwidths required for wireline, only low-oversampling ΣΔMs are actually feasible. This poses an important design challenge, because as the oversampling ratio (M) decreases, the robustness of ΣΔMs decreases as well. In fact, low-oversampling modulators are more sensitive to circuit errors (noise, non-linearity, leakage, mismatching, ...) and, if low M involves high-order filtering, more prone to instability. Hence, careful design is mandatory in order to compete with the Nyquist approach.

This paper discusses architecture and circuit considerations for high bandwidth wireline ΣΔMs beyond ADSL in deep-submicron CMOS technologies.

2. EXPANDIBLE CASCADE MULTI-BIT ARCHITECTURE

Fig.1 shows the block diagram of for an easily expandible, modular family of high-order cascades. It is a Lth-order modulator formed by a second-order stage followed by $L-2$ first-order stages (2-1^{L-2} ΣΔM). The values of the integrator weights are:

$$g_{1a} = g_{1a}' = 0{,}25 \qquad g_{1b} = 1,\ g_{1b}' = 0{,}5$$
$$g_k = 1,\ g_k' = 0{,}5,\ g_k'' = 0{,}5 \qquad k = 2, \ldots, L-1 \tag{1}$$

The last-stage quantization error is shaped by a Lth-order function, the non-linearity error of the last-stage DAC is shaped by a (L-1)th-order function, and there is a systematic DR loss of 6dB − independent of the number of stages. Moreover, Fig.1 shows a constant overloading point (at −5dB), regardless of the number of stages.

This architecture is degraded by opamp finite DC gain and capacitor mismatch. To the purpose of illustration, Fig.2(a) shows the simulated half-scale *SNDR* as a function of the OTA DC-gain for $M = 16$. Also, Fig.2(b) shows the *SNDR* histograms obtained assuming 0.1% sigma in capacitor ratios. Under these conditions, mainly because of the matching sensitivity, the 7th-order architecture is not worth implementing. Nevertheless, the 6th-order modulator provides 90dB worst-case *SNDR* with DC-gain of 2500. Especially robust is the 5th-order cascade requiring a DC-gain of 1000 (only at the first stage opamp) to achieve 80dB worst-case *SNDR* with $M = 16$.

In practice the number of bits in the last-stage quantizer cannot be arbitrarily large. Actually, for given oversampling ratio, the effective resolution saturates as B increases, due to leakage. However, the oversampling ratio reduction that can be achieved by resorting to multi-bit

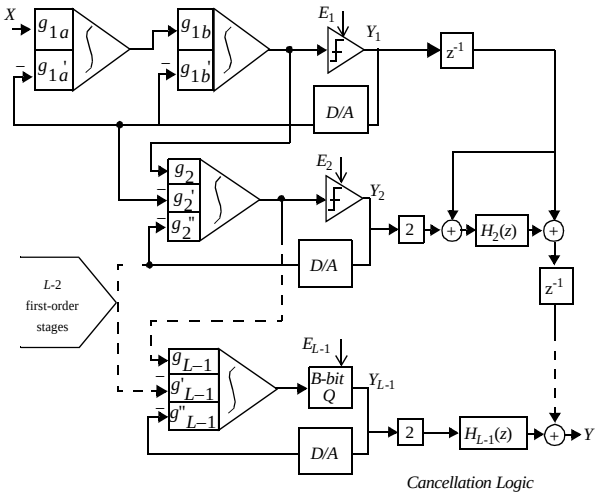

Figure 1. Lth-order ΣΔ modulator using a 2-1^{L-2} cascade.

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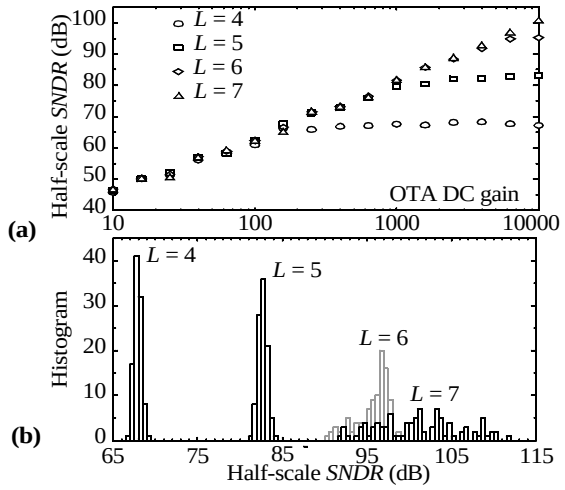

Figure 2. Effect of (a) finite DC-gain and (b) weight mismatch on the *SNDR* of single-bit 2-1^{L-2}ΣΔMs for $M = 16$.

quantization may define the border between feasible and infeasible implementations. Towards this end, proper selection of the main design parameters (L, M, and B) is the key for really efficient implementations.

3. DEEP-SUBMICRON CONSIDERATIONS

3.1 Dominant error mechanisms in high-frequency SDMs

In the presence of circuit imperfections, the dynamic range (*DR*) of a ΣΔM can be approximated by [9],

$$DR \approx 3 \cdot 2^{2ENOB-1} \cong \frac{V_r^2/2}{P_Q + P_{Th} + P_{St}} \tag{2}$$

where V_r is the full-scale input range of the modulator (equal to the reference voltage) and P_Q, P_{Th}, and P_{St} are the in-band powers of the quantization error, thermal noise, and incomplete settling error, respectively. Equilibrium among them, so that $P_Q \approx P_{Th} + P_{St}$, underlies any properly designed ΣΔMs.

Increasing V_r enhances the resolution. Such increase is constrained by the supply voltage and depends on the OTA used at the integrator and on its capability to trade open-loop DC-gain, speed and output swing [10]. An empirical upper bound for V_r is given by:

$$V_r = V_{\text{supply}} - n_{ob} V_{sat}, \text{ in volt-peak differential,} \tag{3}$$

where V_{sat} is the saturation voltage of the output devices and n_{ob} is the number of transistors in the output branch. In the case of the folded-cascode OTA it is $n_{ob} = 4$, thus resulting into a ridiculously small value for the reference voltage. As an alternative, two-stage OTAs [10] may contain only two transistors in their output stages ($n_{ob} = 2$) still producing a large open-loop DC gain.

Let us assume by the time being that the incomplete settling error can be controlled by design so that $P_{St} \ll P_Q, P_{Th}$. A close expression for P_Q is:

$$P_Q \cong \sigma_{mQ}^2 d^2 \frac{\pi^{2L}}{(2L+1)M^{2L+1}} + \sigma_{INL}^2 d^2 \frac{\pi^{2(L-1)}}{(2L-1)M^{2L-1}} + \sigma_{sQ}^2 \left(\frac{25}{48} \frac{\pi^2}{A_v^2 M^3} + 24\sigma_C^2 \frac{\pi^4}{5M^5} \right) \tag{4}$$

where A_v is the first-stage OTA DC-gain, σ_C is the standard deviation associated to capacitor mismatch, and,

$$\sigma_{mQ}^2 = \left(\frac{2V_r}{2^B - 1} \right)^2 / 12 \qquad \sigma_{INL}^2 = \frac{(2V_r \times INL)^2}{2} \qquad \sigma_{sQ}^2 = \frac{(2V_r)^2}{12} \tag{5}$$

are the powers of corresponding errors.

Regarding P_{Th}, it is usually dominated by white noise. Other noise sources, such as $1/f$ noise, play a secondary role, the reason being twofold: (a) DC and the low-frequency region of the spectrum are normally out of the signal band in telecom applications; (b) the usage of small capacitors, in order to relax dynamic requirements, makes kT/C noise dominate over flicker noise. A conservative expression for the in-band power of thermal white noise is [9]:

$$P_{Th} \cong \frac{16kT}{3MC_s} \tag{6}$$

where C_s is the value of the sampling capacitor.

3.2 Estimation of the power consumption

Previous equations show that the *DR* can be expressed as a function of: V_{supply}, L, M, C_s, A_v, and σ_C; plus B and INL if the last-stage quantizer is multi-bit. So, for given values of A_v, σ_C, and INL, the minimum value of C_s required to obtain a given DR can be obtained as a function of M, L, and B. Once C_s is known, the equivalent OTA load for the integrator is,

$$C_{eq} \cong C_s + C_p + C_l \left(1 + \frac{C_s + C_p}{C_o} \right) \tag{7}$$

where C_o, the integrator feedback capacitance, is related to C_s through the integrator weight, $C_o = C_s / g_i$; and C_p, C_l stand for the integrator summing node and output parasitics, respectively. Estimating the latter two capacitances is difficult task because they are largely dependent on the actual OTA design.

The main contribution to C_p is the OTA input parasitics. In a fully-differential topology, this is formed by the input transistor gate-to-source capacitance C_{gs} (both channel and overlap contributions) and its overlap gate-to-drain capacitance C_{gd}^{ov} amplified by Miller ef-

fect. Thus, neglecting C_{gb},

$$C_p \cong C_{gs}^{\text{ch}} + C_{gs}^{\text{ov}} + C_{gd}^{\text{ov}}(1 + A_{v1}) = \frac{2}{3}C_{ox}'W_{in}L_{in} + C_{ox}'W_{in}\Delta L_{in}(A_{v1} + 2) \quad (8)$$

where C_{ox}' is the gate oxide capacitance density, and ΔL_{in} stands for the lateral diffusion of drain/source regions below the gate. Apart from the input transistor dimensions (W_{in}, L_{in}) the other unknown variable in eq. (8) is its input-to-output gain A_{v1}. This equals the total gain of single-stage amplifiers, and the first-stage gain of multi-stage topologies. It can even be around unity if cascode devices are used, such as in folded- or telescope-cascode OTAs [10]. Now, making use of the well-known (as much as inadequate) square-low expression for the input transistor drain current,

$$C_p = \frac{2L_{in}I_{D,in}}{\mu V_{OVD}^2}\left[\frac{2}{3}L_{in} + \Delta L_{in}(A_{v_1} + 2)\right] \quad (9)$$

where $V_{OVD} \equiv V_{GS} - V_T$ is the transistor overdrive.

The other unknown capacitance in (7), C_l, has two main contributions: the first one is due to the bottom parasitic of the integration capacitor C_o; and the second one is due to the OTA itself. The former contribution can vary a lot, depending on the type of capacitors. With modern M-i-M structures it turns out to be very small, ranging from less than 1% to 5% of C_o. Because of this, C_l tends to be dominated by the OTA output parasitic load, which strongly depends on the actual output devices and, overall, on the OTA topology. Even the supply voltage, via output swing and DC-gain requirements, makes an impact on the transistor sizes and hence on C_l. For a given OTA schematic, the latter influence makes C_l slightly increase as supply voltage is reduced, because wider output devices are required to accommodate similar output swings. All things considered, a reliable estimation of this capacitance prior to sizing the OTA is not possible. Based on previous design experiences, we will assume a constant value equal to 2.5pF.

Let us return to the settling error power, P_{St}. We assume that the slew-rate of the OTA is large enough and the switch on-resistance small enough to neglect their impact on the integrator transient response, so that the settling is linear with time constant equal to C_{eq}/g_m. In such case, it takes a number $\ln(2^{ENOB})$ of time constants to settle within *ENOB* resolution; that is, the following relation should be fulfilled:

$$\ln[2^{(ENOB+1)}]C_{eq}/g_m \le T_S/2 \quad (10)$$

where T_S is the sampling period. Note that we have added an extra bit in order to make room for the inaccuracy of this simplified model. The above expression can be used to estimate the minimum value of the transconductance parameter,

$$g_m = 2f_S\ln[2^{(ENOB+1)}]C_{eq} \quad (11)$$

where $f_S \equiv 1/T_S$ is the sampling frequency. This is the transconductance required for a single-stage OTA, for which C_{eq} in eq. (7) is the equivalent output load. For multi-stage OTAs, relation above must be carefully tackled because both parameters, total transconductance and equivalent output load, lose control of the amplifier dynamics. However, provided that the main pole of the OTA is set by the input stage and an eventual inter-stage compensation capacitor, eq. (11) can still be used to determine the input stage transconductance that is related to the input transistor current as:

$$g_m = \frac{2I_{D,in}}{V_{OVD}} \quad (12)$$

Equations (7), (9), (11), and (12) can be handled in an iterative manner to determine the current required through the input transistors of the OTA, whose actual topology sets the power consumption. Whenever possible, a single-stage OTAs should be used for its better performance/power figure. However, as discussed previously, as technologies scale down and supply voltages shrink, two-stage OTAs are gaining ground. Moreover, in practice two gain stages are not enough to achieve the overall gain requirement, so that the first one often includes cascode devices in a telescope cascode configuration [10]. Let's consider this topology as an archetype in modern deep submicron technologies. The current through the first stage has been already estimated as $2I_{D,in}$. Assuming for the sake of simplicity a fixed ratio η_{io} between the currents flowing through the input and output branches, the total current through the OTA can be estimated as,

$$I_B \cong 2I_{D,in} + 2\eta_{io}I_{D,in} + I_{D,in} = [2(1 + \eta_{io}) + 1]I_{D,in} \quad (13)$$

where an extra $I_{D,in}$ has been added to account for the current used in the OTA biasing stage.

With eq. (13) the power dissipation of the first OTA can be estimated. That of the remaining OTAs in the cascade can be made smaller by following the scaling rule commonly applied to the amplifier requirements in ΣΔMs. This power reduction is the outcome of a relaxed set of specifications, and/or the subsequent amplifier topology simplification. Sometimes, even when a two-stage OTA may be required for the first integrator, it is possible to use a single-stage topology for the second and successive integrators. So, we can write

$$I_{B,total} = I_B\left(1 + \sum_{i=2}^{L}\chi_i\right) \quad (14)$$

where χ_i is the ratio between the current absorption of the *i*-th OTA and the first one. From this, the static power dissipated in the OTAs amounts to,

$$P_{op,\,\mathrm{sta}} = I_B V_{\mathrm{supply}} \left(1 + \sum_{i=2}^{L} \chi_i \right) \tag{15}$$

Apart from the static consumption in the OTAs, which usually accounts for 80% of the total power, there are other contributing blocks, namely:

- $L-1$ latched comparators used as single-bit quantizers, and those forming the last-stage multi-bit quantizers, usually implemented by a flash A/D converter, i.e. (2^B-1) more latches. This consumption must include the static power dissipated in a convenient pre-amplifying stage.
- Last-stage multi-bit DAC (if $B>1$). The relaxed requirements for this block allows us to implement it with a resistor ladder. Its main design considerations are resistor matching and linearity (both causing *INL*), and the fact that it must drive enough current to provide a good settling. The current requirement scales with the sampling frequency and the capacitive load involved. The latter can be considered almost constant because the last-stage capacitors should be set to the minimum required to achieve certain level of matching (thermal noise playing a secondary role). So, we can empirically write:

$$P_{DAC} \cong V_{\mathrm{supply}} I_{DAC,\,\mathrm{ref}} \times \frac{f_S}{f_{S,\,\mathrm{ref}}} \tag{16}$$

  where $I_{DAC,\,\mathrm{ref}}$ is the current through the resistor ladder DAC required for operating at a certain frequency of reference, $f_{S,\,\mathrm{ref}}$.
- Dynamic power in SC stages. The dynamic power dissipated to switch a capacitance C_u between the reference voltages at a frequency f_S can be estimated as $C_u f_S V_r^2$, which tends to increase in high-speed, high-resolution converters. Its actual value depends on the integrator weights used. In our case, the following expression provides a good estimate:

$$P_{SC} = 2 \times [5C_{u1} + 4(L-1)C_{u2}] f_S V_r^2 \tag{17}$$

  where the factor 2 applies to differential circuits; C_{u1} is the unitary capacitor used in the first integrator, whereas C_{u2} is the one used in the second and following integrators, usually smaller than C_{u1}.
- Small digital blocks: flip-flops, gates, cancellation logic, etc. Apart from being small, they do not make any difference for the architectures considered, and will be neglected here. Of course, this does not apply to the decimation filter, whose power consumption is comparable to that of the modulator. Moreover, since the order of the digital filter must equal $L+1$, high-order ΣΔMs require more complex filters than low-order ones. However, an increase of the modulator order entails a decrease of the oversampling ratio, the filter can be operated at a lower frequency and dissipates less power. To our purpose, we can consider an essentially constant decimation filter power consumption.

By adding up all the contributions, the power dissipation of the ΣΔM can be estimated by,

$$\begin{aligned} P_{sta} &\cong P_{op,\,\mathrm{sta}} + \\ &+ P_{DAC} + [(L-1) + (2^B-1)] P_{comp} + P_{SC} \end{aligned} \tag{18}$$

4. COMPARISON AMONG CASCADE ARCHITECTURES

he following figure-of-merit (*FOM*) is used to the purpose of comparison,

$$FOM = \frac{Power}{2^{ENOB} \times DOR} \times 10^{12} \tag{19}$$

where *DOR* stands for the digital output rate, i.e., the Nyquist rate.

In a first comparison step, the triads {*L*, *M*, *B*} describing a specific cascade have been evaluated along the curve in the resolution–speed plane shown in Fig.3 (dashed line). Although this particular resolution–speed relationship is arbitrary, it fits the usual requirements for wireline telecom ADCs: ISDN, ADSL, VDSL, etc., which have been placed in the figure for illustration. For each section of the resolution–speed curve, the architecture with the minimum *FOM* has been noted down. Observe that the oversampling ratio decreases as the output rate increases and, simultaneously, the multi-bit quantization shows up to compensate for the oversampling re-

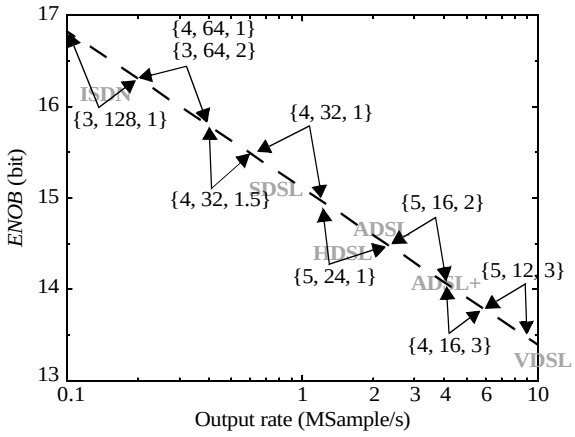

Figure 3. Most efficient cascade ΣΔM for each region of the resolution - speed plane.

duction.

In a second step, we take advantage of the fact that some technology features enter the above formulation to forecast performance evolution of cascade ΣΔMs with technology changes. Fig.4 shows the estimated evolution of the *FOM* of three cascade topologies, namely {4, 24, 1}, {5, 16, 1.5} and {4, 16, 3}, aimed at obtaining 14bit at 4.4MS/s. These are typical specifications for ADSL+ modems. Two facts are noticeable:

- Despite the reduction of the supply voltage, overall, the power dissipation does not decrease below 0.18μm. This is basically due to the reduction in supply voltages, which imposes a reduction in the reference voltage and, hence, the signal power. In order to keep the effective resolution, this loss of signal power must be compensated by an equivalent reduction of the noise power, which can be achieved by increasing the sampling capacitors. Since the incomplete settling error power must be kept constant, the larger the capacitances, the more demanding the dynamic requirements for the OTAs. Whereas up to 0.18μm the increase in current absorption caused by this mechanism is compensated, in terms of power, by the supply voltage scaling, the estimated trend is exactly the opposite below that technology. Once again, the location of the inflection point depends on the converter specifications. For instance, if for the same speed, the resolution is to be increased, the inflection point moves to the right in Fig.4.
- Another aspect illustrated in Fig.4 is the dynamic nature of the architecture selection in Fig.3. Note the evolution of the {4, 16, 3} ΣΔM. It outperforms for 0.25μm and above, but it does not below 0.18μm. The reason behind this is that the multi-bit modulator has a fixed amount of power contributed by the last-stage quantizer that is not present in the single-bit implementation ({4, 24, 1} ΣΔM). In addition, the latter takes advantage of the faster technologies to compensate for the increased oversampling ratio with respect to the multi-bit modulator. The fifth-order {5, 16, 1.5} ΣΔM deserves especial attention. If the quality of the M-i-M capacitors is preserved, this architecture will be worth exploring in the coming technologies.

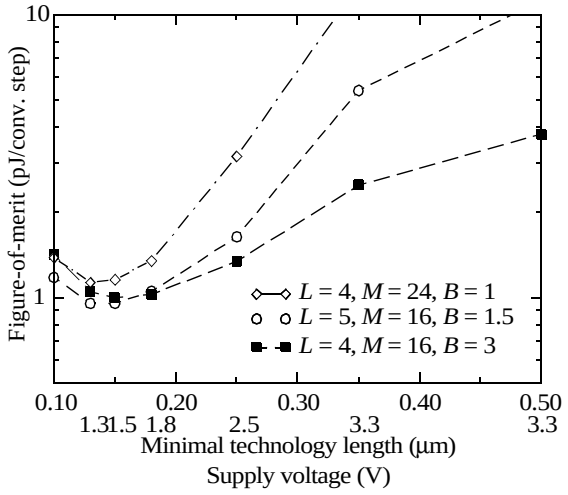

Figure 4. Estimated evolution of the *FOM* with technology for three cascade architectures obtaining 14bit@4.4MS/s.

5. CONCLUSIONS

We have analyzed the performance of family of cascade multi-bit ΣΔMs in deep-submicron. A simple but effective power estimate has been derived, useful for architecture exploration against specification and process changes. It has been shown that, after proper architecture selection, the ΣΔMs here are good candidates for achieving the specifications currently demanded by wireline access technologies. In addition, although process scaling will preclude further power reduction, our conclusion is that some cascade multi-bit ΣΔMs will be worth exploring in 0.13μm and below.

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