ON-LINE CALIBRATION AND DIGITAL CORRECTION OF MULTI-BIT SIGMA-DELTA MODULATORS

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ABSTRACT

In this paper a novel method for the on-line calibration of the DAC used in multi-bit sigma-delta modulators is described. The proposed solution uses an additional transmission zero in the noise transfer function located at half of the sampling frequency. The mismatch between each unity element and a reference is properly modulated and located at the notch position. Since the notch frequency is noise free a simple digital processing allows us to measure mismatches and to store them in a digital memory for digital calibration purposes. The paper shows how to practically implement the above-described approach and discusses a convenient method to attain digital correction. Simulation results verify the proposed technique.

1. INTRODUCTION

One bit noise-shaping sigma-delta (ΣΔ) modulators have achieved great popularity because of their limited accuracy requirement in integrated data converters [1]. The single bit internal DAC is intrinsically linear and does not require precision component matching. Therefore, standard CMOS processes can be used without the need of expensive calibration techniques (such as laser trimming of thin film resistors). However, a sigma-delta modulator achieves high resolution at the expenses of speed. At a certain point, the required oversampling ratio becomes a problem for the active elements used. The resolution improves by increasing the loop filter order or by using cascaded architectures. However, stability issues and the increased complexity of the analog and digital parts limit the benefits.

A possible alternative approach is using a multi-bit quantizer in the oversampling converter loop. A first advantage of this approach is that the ratio of the total quantization noise power to the signal power at the modulator's output is reduced by 6 dB per additional bit in the quantizer. The overall resolution increases accordingly, without requiring to increase the oversampling ratio or use a high order modulator. Therefore, the complexity of the decimation filter (multi-bit in the first stage) diminishes.

Since a multi-bit ΣΔ modulator achieves the same resolution of a single-bit modulator at a lower oversampling ratio, a given technology allows a larger signal bandwidth. Additionally, higher resolution (and hence a reduced quantization noise) provides a significant improvement in the data converter dynamic range.

However, multi-bit ΣΔ modulators require a digital-to-analog converter (DAC) in the feedback loop whose linearity has to be as good as the resolution of the modulator. Non-linearities in the DAC caused by poorly matched components lead to additional noise and spurs. Therefore, methods for precisely matching the components used in the internal DAC become mandatory.

A commonly used technique is the dynamic element matching (DEM) [2, 3, 4]. This method transforms harmonic distortion due to the DAC into wide-band noise, possibly high-pass shaped. A substantial part of the mismatch noise power falls out of the band of interest and is filtered out in the digital domain together with the quantization noise. The DEM technique relies on the capability to transform the mismatch effect into noise. This is not always the case and tones falling in the band of interest may cause a degradation of the spurious-free dynamic range (SFDR). The technique proposed in this paper allows us to avoid this risk. It enables the measurement of component mismatch, thus permitting the digital cancellation of the errors. The accuracy of the mismatch measurement can be as good as desired; therefore, the method allows a full cancellation of the mismatch error.

2. OVERVIEW OF PROPOSED TECHNIQUE

The basic idea behind the proposed technique requires a "clean" frequency in the output spectrum (i. e. with reduced quantization noise). The "clean" frequency is, for instance at half of the sampling frequency ($f_{CK}/2$). A notch in the Noise Transfer Function (NTF) achieves the result.

A second essential element of the method is the use of two additional unity elements in the *DAC*. One of them is used as reference. The second one increases by one unit the *DAC* array so that one element can be periodically calibrated while the remaining *M* perform the normal digital-to analog conversion.

The third constituent of the method is the measurement of the mismatch. We achieve this by introducing a minor addition to the modulator. Fig. 1 shows a modified capacitor based circuit. One element (C_j) of the $M + 1$ unity capacitors is in the calibration mode. It injects a charge equal to $C_j V_{ref}$ every clock cycle in one of the input terminals. On the other terminal the reference branch injects $C_{ref} V_{ref}$. The compensation network cancels the common mode contribution. If the capacitors C_j and C_{ref} are identical the differential signal is not affected. However, if we have a mismatch, a differential term with sign that depends on the sign of the mismatch appears. This term is modulated by a binary signal b_{sc}. Therefore, the measured mismatch corresponds to an additional term superposed to the input signal and the quantization noise. If the modulating bit-stream b_{sc} is a square-wave at $f_{CK}/2$, the mismatch will produce a tone at that frequency.

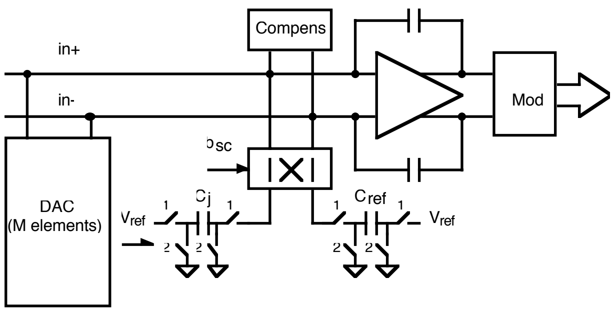

Fig. 1. *Modified modulator for capacitor mismatch measurement.*

The chosen modulation frequency ($f_{CK}/2$) is noise-free. Therefore, the information about mismatch can be easily obtained by a second modulation in the digital domain: the output data stream is multiplied again by a suitably delayed version of b_{sc} and low pass filtered in order to extract the result. Observe that the mismatch is a dc signal. Therefore, after the second modulation it is folded back again to dc. Its value can be measured with the desired precision by simply reducing the bandwidth of the low pass filter used. In practical cases, a digital integrate-and-dump with a very long integration period is good enough for our purposes.

The calibration operation, of course, has to be repeated (if wished periodically in time) for all the *M* components. The information on the difference between each of the $M + 1$ elements of the DAC and the reference one are stored in a look-up table.

To achieve the calibration the mismatch values could be directly added with the digital output before the decimation filter. However, in order to attain the resolution, the mismatch must be very precise and the large number of bits to be digitally processed would greatly increase the digital complexity. Instead, it is more effective to filter the two signals (ΣΔ output bit-stream and mismatch error) independently, and to combine the results after decimation.

3. A/D Converter Implementation

The proposed technique requires to design a ΣΔ modulator including a $(z + 1)$ term in the numerator of the NTF. Moreover, the noise shaping at low frequency must remain unmodified. Finally, the signal transfer function must be flat in the signal band. All, the above features must be obtained without increasing the number of operational amplifiers to be used.

An extensive study of possible architectures leads to the a network that achieves the following Signal Transfer Function (STF) and Noise Transfer Function (NTF)

$$STF(z) = \frac{1.5 + 3.5z}{0.1 + 0.5z + 0.4z^2 + z^3} \quad (1)$$

$$NTF(z) = \frac{(z-1)^2(z+1)}{0.1 + 0.5z + 0.4z^2 + z^3} \quad (2)$$

Therefore, in addition to a notch at $f_{CK}/2$, the ΣΔ modulator transfer function shows, at low frequency, the same noise shaping of a conventional second order modulator.

$$NTF(z)\big|_{z=1} = (z-1)^2 \quad (3)$$

Thanks to the two zeros at dc, and a 4-bit DAC, the resolution achievable is 11 bits at oversampling equal to 16 and 14 bits at oversampling equal to 32.

Fig. 2 shows the output spectrum of the used modulator compared to the conventional one. the spectrum has the same noise shaping at low frequency and displays the required zero at half of the clock frequency.

Fig. 3 shows the architecture that implements the STF and the NTF of equations (1) and (2).

It utilizes two feedback loops with a 4-bit DAC. However only the errors caused by first DAC are important: errors

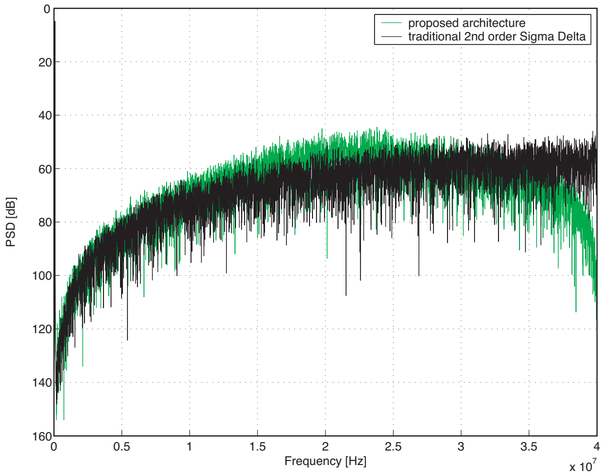

Fig. 2. *Comparison of the spectra of a conventional and the proposed modulator*

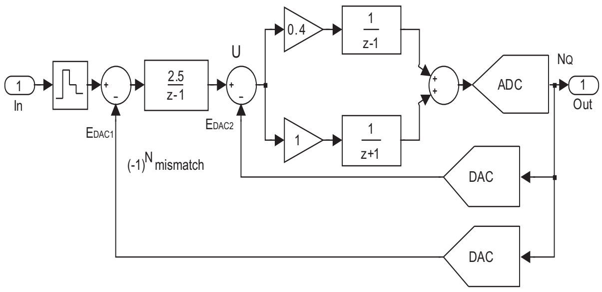

Fig. 3. *Proposed Sigma Delta modulator*

introduced by second DAC, in fact, become negligible because of the first order shaping. Therefore, we assume to use the proposed method only for the first stage.

During the calibration phase the data converter output is

$$Out = In \cdot STF + E_{DAC1} \cdot STF + E_{DAC2} \cdot ETF$$
$$\ldots + N_Q \cdot NTF + (-1)^N \cdot Mismatch \cdot STF \quad (4)$$

where E_{DAC1} represents the error introduced by first DAC, E_{DAC2} the error caused by the second, *ETF* is the Transfer function from node *U* to the *Output* and N_Q is the quantization noise.

Therefore, being the input signal band limited, the output spectrum contains two components: one in the baseband, due to $In \cdot STF(1) + E_{DAC1} \cdot STF(1)$ and one, caused by $(-1)^N \cdot Mismatch \cdot STF(-1)$, at high frequency.

Fig. 4 shows the spectrum obtained with a 0.1% mismatch among the DAC capacitors. Non-linearity in the DAC causes, as expected, harmonic distortion and an increase of the noise in the baseband due to intermodulation of high-frequency components. As discussed the

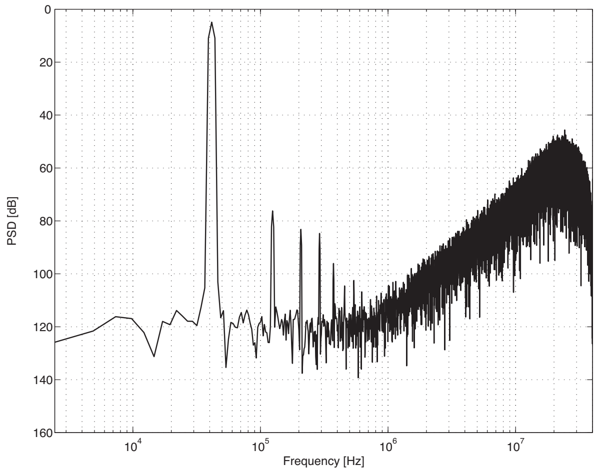

Fig. 4. *PSD of proposed Sigma Delta modulator with mismatch among internal DAC capacitors*

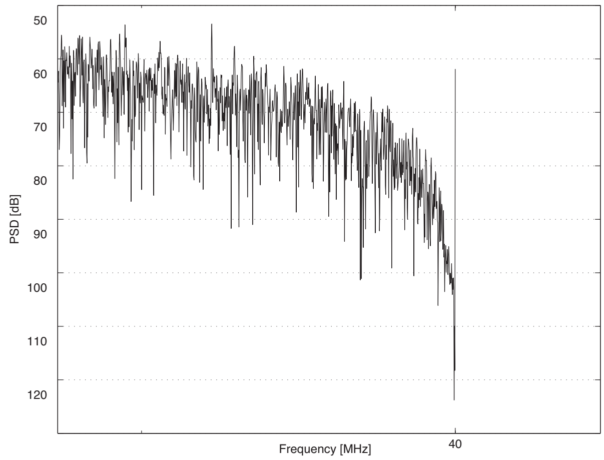

Fig. 5. *Expanded view of Fig. 4, showing the tone at* $f_{CK}/2$

mismatch can be extracted multiplying the output stream by ± 1 .

We achieve mismatch correction in the digital domain by subtracting from the output the estimated mismatch multiplied by the STF. Assuming that the estimation differs from the real error by $Q_{\langle EDAC1 \rangle}$ we have

$$In \cdot STF + E_{DAC1} \cdot STF - \langle E_{DAC1} \rangle \cdot STF = \ldots$$
$$\ldots = In \cdot STF + Q_{\langle EDAC1 \rangle} \cdot STF \quad (5)$$

Therefore, if we want to make the residual error smaller than the quantization contribution it is necessary to use a very accurate estimation of E_{DAC1}.

Fig. 6 shows the schematic of the digital correction hardware. It uses two separate decimation paths for the output ΣΔ bitstream and for the mismatch. It includes the following basic blocks:

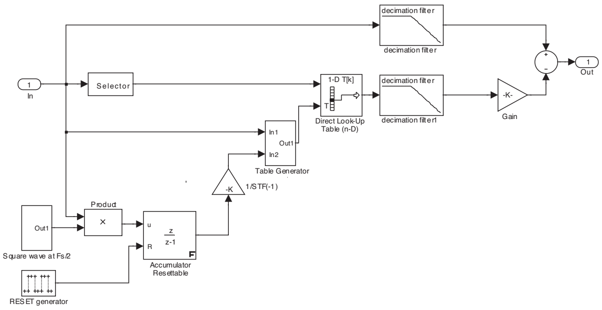

Fig. 6. *Principle scheme of the proposed digital correction hardware*

- a multiplier by ± 1 , synchronized with b_{sc}, to flip the spectra components around $f_{CK}/2$;
- a digital integrator with reset, which achieves the low pass filter function;
- a look-up table, in which the mismatch information is stored;
- the selector block, that based on the $\Sigma\Delta$ modulator output and the element under calibration selects the error;
- the two decimation filters;
- the sum block at the decimation filter output.

The error word-length in the look-up table depends on the expected mismatch between elements. In order to optimize the look-up table dimension is useful to have, for the technology used, an estimation of the expected accuracy. Assuming a mismatch of 0.2%, only four bits words are required for achieving the expected accuracy (14 bit). The considered implementation uses four bit DACs. Therefore, the size of the used memory is pretty small.

The expected matching also determines the integration time of the digital integrator with reset. Simulation results show that using 2^{15} clock periods is more than adequate for our system. Therefore, we complete an entire calibration cycle within 2^{19} clock periods.

The additional hardware in the analog section is very limited: only two additional capacitors are required; moreover, some minor modifications in the driver circuitry allow the capacitors mismatch measurement.

4. Simulation Results

Fig. 7 compares the output spectra with and without calibration. The mismatch between capacitors is 0.2%; the spectra are obtained after decimation (the oversampling ratio is 32). We can observe that harmonic tones as high as –80 dB are completely removed in the calibrated output. Moreover, the noise floor is lowered since the white component of the mismatch is cancelled out.

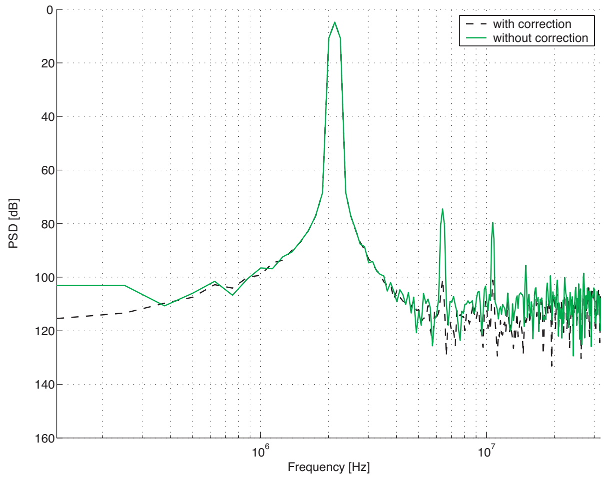

Fig. 7. *Output spectrum of the Sigma Delta modulator (after decimation) with and without calibration*

5. Conclusions

A novel method for the on-line calibration of the DAC used in multi-bit sigma-delta modulators has been described. The method benefits from an additional transmission zero, located at $f_{CK}/2$, in the noise transfer function. This creates a “clean” area in the output spectrum where it is possible to allocate a tone, of amplitude proportional to DAC elements mismatch. A simple digital processing allows us to measure the mismatches and to store them in a digital memory. The paper has shown that a suitable modification of a second order modulator leads to a transmission zero at $f_{CK}/2$ without degrading the noise shaping response. Behavioral simulations validate the proposed technique. Results show that a –80 dB of SFDR are improved by more than 20 dB.

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