MOSFET-ONLY 3^{RD}-ORDER Σ-Δ MODULATORS

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ABSTRACT

The linearity of higher order Σ-Δ modulator using MOSFET capacitors is examined. Two 3^{rd}-order network structures are investigated. For low-voltage power supplies with reference voltages under 1 volt, the performance of a MOSFET-only modulator is predicted to be very close to that of a modulator using linear capacitors. It is possible to realize similar performance in selected modulator network structures. We investigate the performance of a 2-1 cascade and a 3^{rd}-order iflf topology in a $0.35\mu m$ process.

1. INTRODUCTION

The realization of linear, analog circuits using area-efficient capacitors formed by MOS transistor gates becomes important as feature sizes continue to shrink. Sub-micron CMOS technologies suitable for fabricating high speed analog components range from $500nm$ to $120nm$. These technologies offer many possibilities for mixed-signal integrated circuits. It is possible to fabricate an entire analog-to-digital converter (ADC), digital post filters and digital electronics on a single die. Linear capacitors are required in order to implement analog filters, switched-capacitor filters and sigma-delta analog-to-digital converters (ADC)s. Since these processes are tailored for digital circuits many do not offer a second poly layer, eliminating the most common type of linear capacitor.

Realizing capacitors from MOS transistor gates is an attractive option. Other alternatives include MOS capacitors with heavily doped channels or poly-metal capacitors. MOS transistors with heavily doped channels require additional processing steps which are not available in many digital IC technologies. Poly-metal capacitors typically consume a great deal more area than poly-poly capacitors. This is due to the greater oxide thickness. Poly-metal capacitors can also be realized with an additional metal layer, e.g. poly-metal-metal; but this is not always possible. Due to the larger area and surface issues between oxide and deposited aluminum matching errors also increase using metal for one or more capacitor plates. MOS capacitors are readily available in a CMOS process and provide an order-of magnitude improvement in area efficiency over a poly-metal capacitors. As transistor gate dimensions are scaled the oxide thickness is reduced thereby increasing the oxide capacitance as feature sizes are reduced; however, the gate capacitance varies with the node voltages making the device nonlinear. Hence, MOS capacitors need to be linearized, and the added circuitry can dramatically reduce the advantage in area-efficiency cited earlier.

There are attractive methods available to fabricate MOS capacitors. The nonlinear relationship with voltage can be minimized by placing two MOS capacitors in series allowing the nonlinearities to cancel each other. This approach is known as series compensation[1, 2]. MOS capacitors can be formed in either the inversion region or the accumulation region, fully exploiting the thin oxide, alternatively, a capacitor can also be formed in the depletion region. Two linearizion methods using series compensation have been proposed: (1) operating the transistors in the accumulation region[1] and (2) operating the transistors in the depletion region[2]. The former requires a bias voltage larger than the supply voltage of the circuit while the latter can be made to be self-biasing, making it attractive for lower voltage power supplies in sub-micron integrated circuits despite being less area efficient.

This paper presents analysis and simulation results for two 3^{rd}-order modulator network structures, the 2-1 cascade[3, 4] proposed by Ribner and the 3^{rd}-order iflf[5] proposed by Fergusson et. al..

2. SERIES COMPENSATION OF DEPLETION MODE MOS CAPACITORS

This approach has been proposed by Tille, et. al.[2] and the schematic illustrating the series compensation and biasing is shown in figure 1. Two p-channel transistors M1 M2 form the capacitor. The wells of each transistor form the top and bottom plate of the capacitor. The terminals for the series connection are the well contacts, thus, this is intended for an N-well process which is most popular today. The series connection is made between the gates of the two transistors. The sources and drains are tied together to V_{ss} to avoid forward biasing drain or source terminals. The 3^{rd} transistor, M3, provides the biasing of the gate. It operates in the sub-threshold region and prevents charge build up at the gate connection between M1 M2. A diagram of the technique proposed by Tille[2] is shown in figure 2. Only the source terminal of M3 is shown (as the N^+ contact). The dimensions of M3 must be kept small to minimize parasitic capacitance on the implementation[2].

The the only parasitic capacitance results from the p-n junction formed by the p-substrate and the n^+ contact. The equivalent circuit is shown in figure 3. Thus there is little capacitance other than the charge between the top and

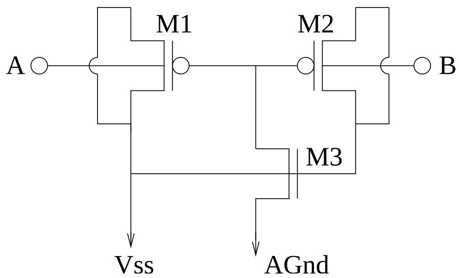

Fig. 1. Series compensation scheme proposed by Tille et. al.[2].

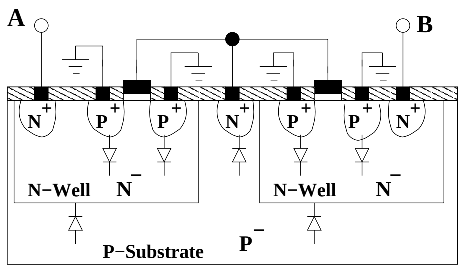

Fig. 2. MOS capacitor realized from series connected PMOS transistors.

bottom plate. There is a non-zero leakage current between the wells (which form the top and bottom plates); fortunately it is in on the order of a few nA and it appears only when there is a high gate-body voltage. Thus, the leakage current is negligible.

3. PROCESS COMPARISON

Typically, the Gate-Body capacitance of an enhancement mode MOS transistor is much larger when it is in the inversion or accumulation regions when compared to operation in the depletion region. In the depletion region the capacitance is smaller due to the widening of the depletion layer. As the gate oxide thickness decreases the difference between MOS capacitance in accumulation/inversion and depletion decreases. C_{ox}, the Gate-Body capacitance per unit area is inversely proportional to the depth of the depletion region. The depth of the depletion region under the channel is given by[2, 6]

$$d_{Depl} = \frac{\epsilon_o \epsilon_{Si}}{C_{ox}} \left(\sqrt{1 + \frac{2|V_{GB} - V_{FB}|C_{ox}^2}{\epsilon_o \epsilon_S i q N_{Sub}}} - 1 \right) \quad (1)$$

where the product, $\epsilon_o \epsilon_{Si}$, is C_{ox} is the Gate-Body capacitance per unit area, V_{GB} is the Gate-Body voltage, V_{FB} is the Flat-Band voltage, q is the charge of an electron and N_{Sub} is the substrate doping concentration.

HSPICE simulations[6–8] have been performed for the circuit in figure 2 using BSIM3 parameter sets for several sub-micron CMOS processes, a $0.35\mu m$, a $0.25\mu m$ and a $0.18\mu m$. These results are summarized in figure 4 and table 1. The oxide thickness is on the order of $10\mathring{A}$-$100\mathring{A}$.

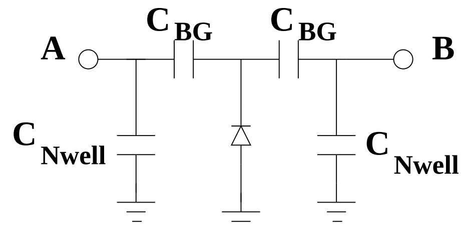

Fig. 3. Equivalent circuit from figure 2.

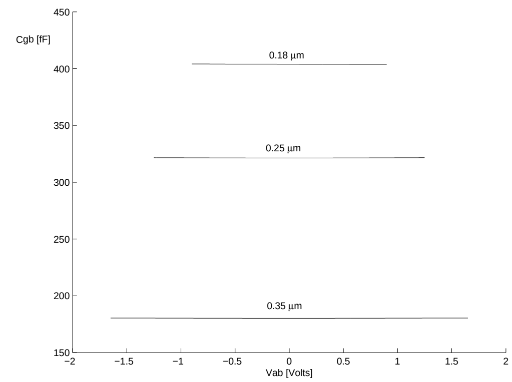

Fig. 4. Linearity of series compensated MOS capacitors over several sub-μmeter process technologies.

The results presented in figure 4 were simulated using $W = L = 20\mu m$ for each transistor simulated. This yields a variation of less than 0.2% for any of the processes over a 1 volt range. In table 1 we see a typical oxide thickness and a comparison between the unit capacitance for metal-poly, poly-poly and series-compensated depletion mode MOS capacitors. Please note that the superscript 1 indicates that the unit capacitance of the poly-poly capacitor is estimated since a second poly layer is not available in the $0.25\mu m$ process and the $0.18\mu m$ process.

IC Process	t_{ox} [$\mathring{A}$]	Metal-Poly Cap [$\frac{aF}{\mu m^2}$]	Poly-Poly Cap [$\frac{aF}{\mu m^2}$]	Ser-Con MOS-C [$\frac{aF}{\mu m^2}$]
$0.35\mu m$	78	200	912	225
$0.25\mu m$	57	200	$1,000^1$	402
$0.18\mu m$	42	200	$1,200^1$	505

Table 1. Process Comparison[1].

4. 3^{RD}-ORDER MODULATORS

There are four common single-bit 3^{rd}-order modulator network structures[9]:

a) the iflf3 (inverse follow-the-leader feedback), which is a single stage modulator consisting of a cascade of 3 integrator stages; the output of the 3^{rd} integrator is fed into the quantizer; quantization noise is fed back to each integrator input.

b) the flf3 (follow-the-leader feedback), which is a single stage modulator consisting of a cascade of 3 integrator stages; the integrator outputs are summed and fed-forward into the quantizers; quantization noise is fed back to the 1^{st} integrator input.

c) 2-1 cascade, mod21, which is a cascade of a 2^{nd}-order modulator and a 1^{st}-order modulator.

d) 1-1-1 cascade or MASH, which is a cascade of 3 1^{st}-order modulators.

We selected two network structures: the mod21 and the iflf3. The MASH is not very useful for this application. At least a 2^{nd}-order modulator is required for the 1^{st}-stage in a cascaded modulator implementation (assuming non-linear coefficients). The flf3 requires an analog summing amplifier and we have chosen to avoid this additional complexity.

The first network structure is composed of a cascade of a 2^{nd}-order loop and a 1^{st}-order loop, the 21-Modulator, proposed by Ribner[3]. The block diagram of this modulator is shown in figure 5. Analog subtraction is not performed in Ribner's approach. Instead, the quantizer input signal from the first stage is fed into the second stage and the subtraction required for the noise-cancellation is performed in the digital domain[3]. This network structure displays a high degree of insensitivity to static errors such as finite gain and C-Ratio mis-match errors.

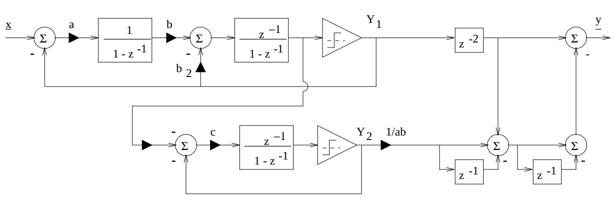

Fig. 5. Block diagram of Ribner's 2-1 modulator.

The second modulator investigated is the 3^{rd}-order structure first proposed by Fergusson[5] et. al.. The block diagram is shown in figure 6. The modulator is realized by 3 integrators in an iflf topology. The biquad allows for the placement of a null in the in-band quantization noise. This modulator is also quite insensitive to gain and matching errors.

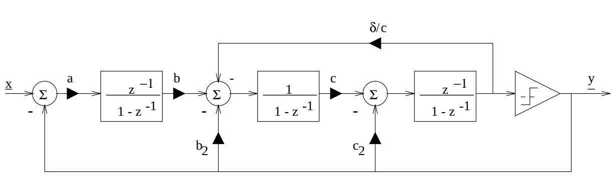

Fig. 6. Block diagram of Fergusson's 3^{rd}-order iflf network.

Simulations were performed to analyze the performance using the DelSi toolbox[10] for the $0.35\mu m$ process. The DelSi toolbox was modified to incorporate voltage dependent C-Ratios for the critical coefficient values. This allows us to compare the performance of a modulator realized with the series connected depletion mode MOS capacitors to one with linear capacitors such as poly-poly caps. The voltage dependence was modeled as a ratio of polynomials, e.g. $C = p(V_n)/p(V_d)$. The polynomial was found by fitting an 8^{th}-order polynomial to the curve for the $0.35\mu m$ process in figure 4. The Signal-to-Noise-Plus-Distortion (SNDR) vs. Signal Power and the Total Harmonic Distortion vs. Signal Power were plotted for each example. The SNDR, THD and Input signal power were estimated using 2^{18} point FFTs averaged 4 times. The 7-Term Minimum Sidelobe window[11] was again employed.

If the reference voltage is higher than 1 $Volt$ the non-linear behavior due to the MOS capacitors is no longer negligible. For example, if we apply $V_{ref} = 1.54$ Volts (which implies a power supply of 4-5 Volts) to the 21-modulator network the performance is significantly degraded for the higher input voltage. This result, which is not surprising, is illustrated in figure 7.

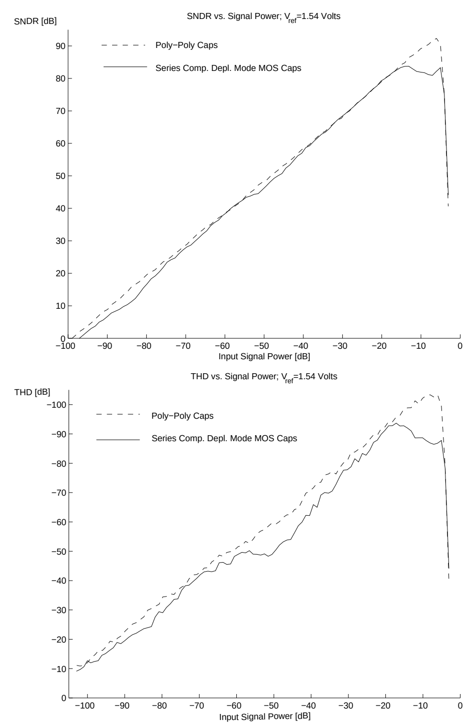

Fig. 7. Comparison of linear and series compensated depletion mode capacitors in the 21-Modulator for $V_{ref} = 1.54V$.

The simulation results for each network structure, with V_{ref}=1Volt, are shown in figures 8 and 9 for the 21-Modulator and the 3^{rd}-order iflf, respectively.

5. SUMMARY

Both the 2-1 network and the iflf3 network results indicate that this approach is feasible for higher-order modulators for low voltage power supplies with reference voltages of 1 Volt or less. We intend to fabricate each modulator presented in this summary. The sub-micron process is a

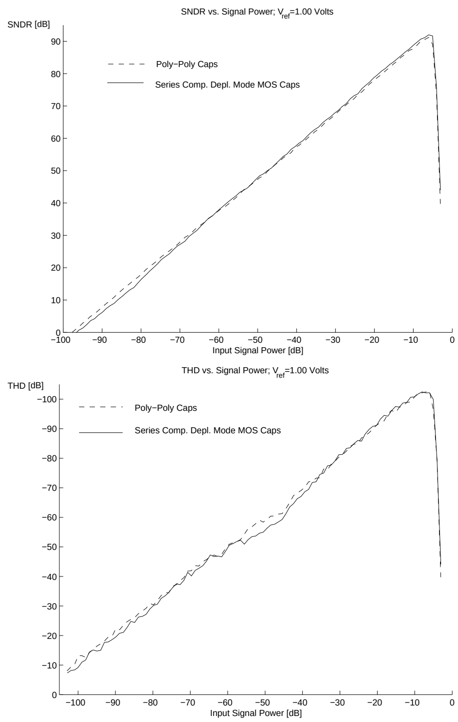

Fig. 8. Comparison of linear and series compensated depletion mode capacitors in the 21-Modulator.

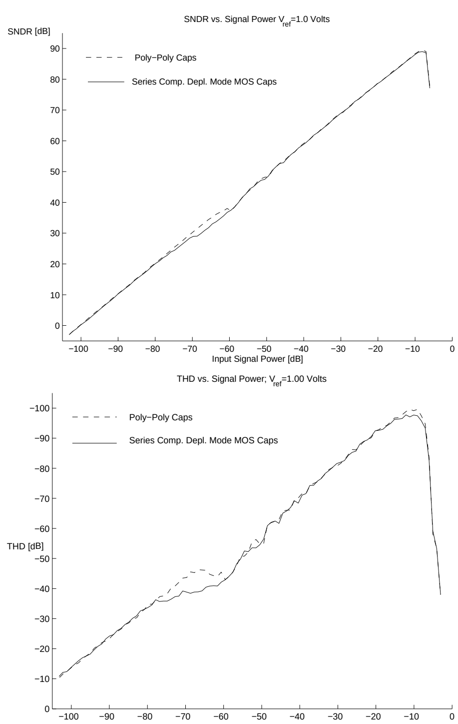

Fig. 9. Comparison of linear and series compensated depletion mode capacitors in the 3^{rd}-order iflf.

$0.35\mu m$ digital CMOS process which provides the option for a 2^{nd} poly layer. This allows us to directly compare the MOSFET-ONLY modulator with its counterpart implemented with poly-poly caps. We believe it is possible to have at least preliminary results for the final paper submission and final results for the presentation at the conference.

6. REFERENCES

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